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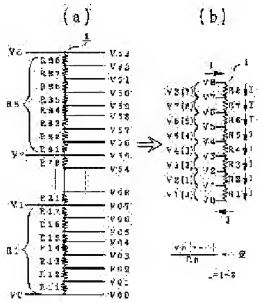
(54) LIQUID CRYSTAL DISPLAY DEVICE



(57)Abstract:
PURPOSE: To reduce the cost of consumed power and to enable high picture quality display by allowing the resistance value between the terminals of a series resistance voltage dividing circuit through which the reference voltage of each tone is applied to be equal to the one proportional to the potential difference between each tone reference voltage.

CONSTITUTION: The tone reference voltage generating circuit generates tone voltages for 64 tones by dividing each interval of the 9 tone reference voltages ranging from V0 to V8 inputted from the internal power source circuit into 8 equal divisions. It is also provided with a switching means which changes the resistance values R1 to R8 between the terminals through which each reference voltage is impressed to the ones proportional to the potential differences Vn(n-1) between each tone reference voltage. As the results, the current flowing through the series resistance voltage dividing circuit 1 becomes constant and the inflow and outflow of current from parts other than the terminals for application of tone reference voltage become mostly none, reducing the power consumption of the drain driver.

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CLAIMS

[Claim(s)]

[Claim 1] The liquid crystal display panel by which two or more arrangement of the pixel which has the pixel electrode electrically connected to the source of a thin film transistor and this thin film transistor was carried out, The drain driver which was chosen as the drain of the above-mentioned thin film transistor from the gradation electrical potential difference of two or more potentials and which outputs an electrical potential difference, The power circuit which outputs the gradation reference voltage of two or more potentials to the above-mentioned drain driver, It is the liquid crystal display which chooses the above-mentioned pixel as the gate of the above-mentioned thin film transistor and which has the gate driver which outputs an electrical potential difference. The above-mentioned drain driver has a gradation electrical-potential-difference generation circuit. The above-mentioned gradation electrical-potential-difference generation circuit Between the potentials of two or more above-mentioned gradation reference voltages is pressured partially to two or more potentials by the partial pressure circuit which connected resistance to the serial. The liquid crystal display characterized by having generated the gradation electrical potential difference of two or more above-mentioned potentials, and setting the resistance between the potentials of each gradation reference voltage of the above-mentioned partial pressure circuit as the resistance mostly proportional to the potential difference between each gradation reference voltage.

[Claim 2] The liquid crystal display indicated by claim 1 characterized by providing the change means for changing the resistance between the potentials of each gradation reference voltage of the above-mentioned partial pressure circuit into the resistance mostly proportional to the potential difference between each gradation reference voltage.

[Claim 3] The liquid crystal display indicated by claim 1 characterized by providing the selection means for preparing two or more series resistance circuits between the potentials of each gradation reference voltage of the above-mentioned partial pressure circuit, and choosing the series resistance circuit used as the resistance mostly proportional to the potential difference between each gradation reference voltage from said two or more series resistance circuits.

[Claim 4] The liquid crystal display panel by which two or more arrangement of the pixel which has the pixel electrode electrically connected to the source of a thin film transistor and this thin film

transistor was carried out, The drain driver which was chosen as the drain of the above-mentioned thin film transistor from the gradation electrical potential difference of two or more potentials and which outputs an electrical potential difference, The power circuit which outputs the gradation reference voltage of two or more potentials to the above-mentioned drain driver, It is the liquid crystal display which chooses the above-mentioned pixel as the gate of the above-mentioned thin film transistor and which has the gate driver which outputs an electrical potential difference. The above-mentioned drain driver has a gradation electrical-potential-difference generation circuit. The above-mentioned gradation electrical-potential-difference generation circuit Between the potentials of two or more above-mentioned gradation reference voltages is pressured partially to two or more potentials by the partial pressure circuit which connected resistance to the serial. If the gradation electrical potential difference of two or more above-mentioned potentials is generated, the potential difference of the one above-mentioned gradation reference voltage Vn and other gradation reference voltage Vn-1 is set to Vn (n-1) and the above-mentioned gradation reference voltage Vn and the combined-resistance value between the impression terminals of the above-mentioned partial pressure circuit of Vn-1 are set to Rn The liquid crystal display characterized by setting up the value of each resistance of the above-mentioned partial pressure circuit so that the value of Vn (n-1)/Rn may be in agreement within the limits of specific fluctuation to all Rn.

[Claim 5] The liquid crystal display indicated by claim 4 characterized by setting up the value of each resistance of the above-mentioned partial pressure circuit so that it may be in agreement to Rn of all above within the limits of the fluctuation whose value of Above Vn (n-1)/Rn is **23%.

[Claim 6] The liquid crystal display indicated by claim 4 characterized by setting up the value of each resistance of the above-mentioned partial pressure circuit so that it may be in agreement to Rn of all above within the limits of the fluctuation whose value of Above Vn (n-1)/Rn is **15%.

[Claim 7] The liquid crystal display indicated by claim 4 characterized by setting up the value of each resistance of the above-mentioned partial pressure circuit so that the value of Above Vn (n-1)/Rn may be completely in agreement to Rn of all above.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the gradation electrical-potential-difference generation circuit of the liquid crystal display in which a multi-tone display is possible especially about the liquid crystal display used for a personal computer, a workstation, etc.
[0002]
[Description of the Prior Art] An example of the TFT-liquid-crystal display in which it is possible, a multicolor display, for example, the multicolor display of 64 gradation, is indicated by the following reference I.
[0003] I "Low-Power 6-bit Column Driverfor AMLCDs"
(June, 1994 issue SID 94 DIJEST P.351-354) .
[0004] Drawing 8 is the block diagram showing the outline configuration of the TFT-liquid-crystal indicating equipment indicated by said reference I.
[0005] In drawing 8 , 800x3x600 pixels (TFT-LCD) of liquid crystal display panels consist of Pix(es).
[0006] The equal circuit of the pixel Pix of a TFT-liquid-crystal display panel is shown in drawing 9 .
[0007] ITO is a pixel electrode, COM is a counterelectrode, and a liquid crystal display component (not shown) is formed in ITO, COM, and a liquid crystal layer.
[0008] When an equal circuit shows a liquid crystal display component, it can be expressed with electrostatic capacity CLC.
[0009] Since the permeability of light changes with the electrical potential differences impressed between ITO and COM as a liquid crystal display component is shown in drawing 14 , a multi-tone display can be performed by impressing the gradation electrical potential difference on

which the electrical potential difference was decided to be the pixel electrode ITO for two or more display gradation of every on the basis of the electrical potential difference impressed to COM.
[0010] Dn is a drain wire or a video-signal line, and a gradation electrical potential difference is impressed to two or more drain wires Dn from the drain driver 11.
[0011] TFT is a thin film transistor, has the drain D electrically connected to the sources S and Dn electrically connected to ITO, and Gate G, and controls the electric flow between Dn and ITO, and un-flowing by the electrical potential difference applied to Gate G.
[0012] Gn is a gate line or the scanning line, and since Gn is connected to the gate G of corresponding TFT of Pixel Pix, the pixel electrode ITO which impresses a gradation electrical potential difference by Gn can be chosen.
[0013] Cadd is retention volume, Cn is a capacity line, and Cadd can be held until the gradation electrical potential difference impressed to ITO is impressed to a gradation electrical potential difference by ITO next.
[0014] Drawing 10 is drawing showing the timing of the voltage waveform impressed to the pixel shown in drawing 9 .
[0015] In (1), the wave of the gate line Gn and (2) show the wave of Counterelectrode COM and the capacity line Cn, and (3) shows the wave of a drain wire Dn in this drawing. When impressing a gradation electrical potential difference to the pixel electrode ITO, it is a gate voltage waveform (1). Gate On It is set to level and between the source of TFT and a drain flows. The drain voltage waveform (3) and the counterelectrode voltage waveform (2) are the form which the phase reversed, and the electrical potential difference of the difference of a drain voltage waveform (3) and a counterelectrode voltage waveform (2) is impressed to the liquid crystal display component CLC. Since the electrical potential difference impressed to the liquid crystal display component CLC has set up the gate voltage waveform (1), the counterelectrode voltage waveform (2), and the drain voltage waveform (3) so that the timing impressed with straight polarity and the timing impressed by negative polarity may appear by turns, a dc component is not impressed to the liquid crystal display component CLC, and it does not have the fall of the life of a TFT-liquid-crystal display panel, the seizure of an image, and the problem of an after-image.
[0016] The description of the liquid crystal display using TFT does not have a cross talk between each pixel Pix in order to impress a gradation electrical potential difference to the pixel electrode ITO through a

switching element called TFT, it does not have the need of using the special drive approach for preventing a cross talk like a simple matrix form liquid crystal display, and is in a multi-tone display being possible.

[0017] Moreover, as shown in drawing 8 , the drain driver 11 is arranged at one liquid crystal display panel (TFT-LCD) side, this drain driver 11 is connected to the drain wire of a thin film transistor (TFT), and the electrical potential difference for driving liquid crystal to a thin film transistor (TFT) is supplied.

[0018] Moreover, a gate driver 12 is arranged in the side face of a liquid crystal display panel (TFT-LCD), and it connects with the gate line of a thin film transistor (TFT), and is Gate to the gate G of 1 level operating-time (1H) thin film transistor (TFT). On electrical potential difference is supplied.

[0019] A display control 10 drives the drain driver 11 and a gate driver 12 for the data for a display and the display-control signal from [from an interface connector] a main frame computer based on reception and this.

[0020] Here, the data for a display from a main frame computer consist of every color bits [6 bits] 18 bits.

[0021] The drain driver 11 has one gradation electrical-potential-difference generation circuit, as shown in drawing 11 , and said gradation electrical-potential-difference generation circuit generates the gradation electrical potential difference for 64 gradation from the gradation reference voltage (V0-V8) of nine values inputted from the internal power circuit 13.

[0022] Moreover, the drain driver 11 incorporates the every color bits [6 bits] data for a display by the output number in an input register with a shift register synchronizing with the clock signal CLK1 for an indicative-data latch. Next, according to the clock signal CLK2 for output timing control, the data for a display in an input register are incorporated to a SUTOREJI register, and out of the gradation electrical potential difference for 64 gradation generated in said gradation electrical-potential-difference generation circuit, an output circuit chooses the gradation electrical potential difference corresponding to the data for a display, and outputs it to each drain wire Dn.

[0023] The polar terminal of the drain driver 11 is prepared in order to control the polarity of the electrical potential difference outputted to a drain wire Dn, and the carry input and the carry output terminal are prepared in order to take cooperation between the drain drivers 11 of the plurality in a liquid crystal display.

[0024] Drawing 12 is drawing showing the gradation electrical-potential-difference generation circuit of the drain driver 11 shown in said drawing 11 .
[0025] As shown in (a) of drawing 12 , the gradation electrical-potential-difference generation circuit of the drain driver 11 shown in said drawing 11 divides into eight equally between each gradation reference voltage of the gradation reference voltage (V0-V8) of nine values inputted from the internal power circuit 13 by the series resistance partial pressure circuit 1, and generates the gradation electrical potential difference for 64 gradation of V00-V63.
[0026]
[Problem(s) to be Solved by the Invention] As shown in drawing 14 , the relation of the electrical potential difference and permeability which are generally impressed to a liquid crystal layer is not linear, there is little change of the permeability to the electrical potential difference impressed to a liquid crystal layer the high place of permeability and when low, and its change of permeability is large in the place used as the middle.
[0027] For this reason, in the liquid crystal display in which the multicolor display of 64 gradation is possible, in order to display 64 gradation on a linear, not regular intervals but near halftone (V2-V6), the gradation reference voltage level given to the gradation electrical-potential-difference generation circuit of the drain driver 11 has a small difference, and it must make it large other than this (V0-V2, V6-V8).
[0028] However, by said reference, how the resistance of the series resistance partial pressure circuit 1 of the gradation electrical-potential-difference generation circuit of the drain driver 11 shown in said drawing 12 is set up has not made reference in detail.
[0029] Therefore, the direct-current (DC) current flowed on the line which will supply gradation reference voltage to it if the gradation reference voltages V0-V8 which are not spacing, such as being shown in drawing 14 , are impressed to the series resistance partial pressure circuit 1 of the gradation electrical-potential-difference generation circuit shown in (a) of drawing 12 , and there was a problem on which power consumption increases.
[0030] For example, although (b) of drawing 12 simplifies this drawing (a) If the resistance between each gradation reference voltage impression terminal of the series resistance partial pressure circuit 1 is made into a fixed value by 100 ohms in a gradation electrical-potential-difference generation circuit, respectively The gradation

reference voltage difference between Vgradation reference voltage V0-1, between VV1-2, between VV6-7, and between VV7-8 becomes twice a gradation reference voltage difference between Vgradation reference voltage V2-3, between VV3-4, between VV4-5, and between VV5-6.

[0031] Therefore, the flowing current between the terminals which impress the gradation reference voltage of the gradation reference voltages V6 and V7 of the series resistance partial pressure circuit 1, and between the terminals which impress the gradation reference voltage of the gradation reference voltages V1 and V2 The current which flows between the terminals which impress the gradation reference voltages V5 and V6 of the series resistance partial pressure circuit 1 and the gradation reference voltage of the gradation reference voltages V2 and V3 is set to 5mA (0.5V/100ohm=5mA) to being 10mA (1.0V/100ohm=10mA).

[0032] Therefore, the current flowed and flowed out of the terminal which impresses the gradation reference voltage V6 of the series resistance partial pressure circuit 1 where a current value becomes discontinuous, and the terminal which impresses the gradation reference voltage V2, and since the current which flows in a gradation electrical-potential-difference generation circuit increased, there was a problem that the power consumption of the drain driver 11 increased.

[0033] Moreover, when the current flowed and flowed out at the line which supplies the gradation reference voltages V1-V7, the increment in the power consumption by the internal resistance of a power circuit 13 was also a problem.

[0034] Drawing 13 is drawing showing the generation section of the gradation reference voltages V0-V8 of a power circuit 13.

[0035] This drawing (a) shows the example which generates the generation section of the gradation reference voltages V0-V8 in a resistance partial pressure circuit. The gradation reference voltages V0-V8 are set up by the ratio of the value of resistance RR0-RR9, and the output of the partial pressure circuit of resistance RR0-RR9 is amplified by sufficient power, and is outputted to the series resistance partial pressure circuit 1 of the drain driver 11 by buffer circuits OP0-OP9.

[0036] This drawing (b) is drawing showing the equal circuit of this drawing (a). A power circuit 13 can be expressed with direct current voltage supplies v0-v8 and internal resistance r0-r8. Direct current voltage supplies v0-v8 are considered that it is decided by the output of the partial pressure circuit of resistance RR0-RR9, and internal resistance r0-r8 is decided by the output impedance of buffer circuits OP0-OP9.

[0037] Supposing it sets internal resistance r0-r8 to 20 ohms, when a

5mA current flows on the supply line of the gradation reference voltage V2, 0.5mW power will be consumed too much in a power circuit 13. Moreover, since the voltage drop of 0.2V is produced with internal resistance r2, the gradation reference voltage V2 outputted to the drain driver 11 also descends 0.2V, and cannot output the gradation electrical potential difference made into the purpose to a liquid crystal display panel, but also produces the problem from which right display gradation is not obtained.

[0038] For moreover, the purpose which simplifies a configuration and makes the chip size of an integrated circuit small in the drain driver 11 If the number of the drain signal line which chooses the same gradation electrical potential difference within one drain driver 11 increases in order to share the output of a gradation electrical-potential-difference generation circuit with all the drain wires that the drain driver 11 drives, as shown in drawing 11 The current which flows to the resistance R1-R8 of the gradation reference voltage generation circuit 1 becomes large. Change each gradation electrical potential difference every drain driver 11, and change of the permeability of the liquid crystal layer to applied voltage especially on the display screen of a large halftone display (V2-V6) The brightness difference occurred on the boundary of the drain wire Dn with which the drain drivers 11 differ, and the pixel Pix corresponding to Dn+1, and there was a trouble that display quality deteriorated.

[0039] Namely, the gradation reference voltage difference V3 (2), V4 (3), when it sees in the example shown in drawing 12 Although V5 (4) and V6 (5) are lower than V1 (0), V2 (1), V7 (6), and V8 (7), since the value of R3-R6 is the same as the value of R1, R2, R7, and R8 It becomes difficult to pass sufficient current for the output line of the gradation electrical potential difference (V15-V47) outputted from the resistance partial pressure circuit between V2 - V6.

[0040] Made in order that this invention may solve the trouble of said conventional technique, the purpose of this invention is in the gradation electrical-potential-difference generation circuit of a liquid crystal display to offer the liquid crystal display which enables a high-definition display with a low power.

[0041] Other purposes and new descriptions are clarified by a publication and accompanying drawing of this specification at said purpose list of this invention.

[0042]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this

application.
[0043] (1) It is the liquid crystal display which generates the multi-tone gradation electrical potential difference which pressures partially between each gradation reference voltage of two or more gradation reference voltages by the series resistance partial pressure circuit, and impresses it to a liquid crystal layer, and is characterized by making into the resistance mostly proportional to the potential difference between each gradation reference voltage the resistance between the terminals which impress each gradation reference voltage of said series resistance partial pressure circuit.
[0044] (2) In the means of the above (1), it is characterized by providing the change means for changing into the resistance mostly proportional to the potential difference between each gradation reference voltage the resistance between the terminals which impress each gradation reference voltage of said series resistance partial pressure circuit.
[0045] (3) In the means of the above (1), two or more series resistance circuits are prepared among the children who do the impression edge of each gradation reference voltage of said series resistance partial pressure circuit, and it is characterized by providing the selection means for choosing the series resistance circuit which serves as resistance mostly proportional to the potential difference between each gradation reference voltage out of said two or more series resistance circuits.
[0046] In the gradation electrical-potential-difference generation circuit of the liquid crystal display which generates the multi-tone gradation electrical potential difference impressed to a liquid crystal layer according to said each means The resistance between each gradation reference voltage impression terminal of a series resistance partial pressure circuit is proportional to the electrical-potential-difference difference between each gradation reference voltage. Among the gradation reference voltage impression terminals of a series resistance partial pressure circuit The inflow of the current from other than the gradation reference voltage impression terminal with which the greatest gradation reference voltage and the minimum gradation reference voltage electrical potential difference are impressed, Most outflows are set to 0, it becomes possible to reduce the power consumption of the drain driver 11 and a power circuit 13, and the power consumption of the whole liquid crystal display can be reduced.
[0047] Moreover, in order that change of the permeability of the liquid-crystal layer to applied voltage may make small the resistance between

gradation reference voltage impression terminals in the part of a large halftone display, even if the number of the drain signal line which outputs the same gradation electrical potential difference increases, the voltage variation of the gradation electrical potential difference of a gradation electrical-potential-difference generation circuit becomes small, it becomes possible to suppress that a brightness difference occurs on the boundary between Pixels Pix where the drain drivers 11 differ, and the display property of a liquid crystal display improves.

[0048]

[Embodiment of the Invention] Hereafter, the operation gestalt of the TFT-liquid-crystal display which applied this invention is explained to a detail with reference to a drawing.

[0049] In addition, in the complete diagram for explaining an operation gestalt, what has the same function attaches the same sign, and explanation of the repeat is omitted.

[0050] Hereafter, since the TFT-liquid-crystal display configuration to which this invention is applied is the same as the TFT-liquid-crystal display shown in said drawing 8 , explanation is omitted.

[0051] [Operation gestalt 1] Drawing 1 is drawing showing the gradation electrical-potential-difference generation circuit of the drain driver 11 of the liquid crystal display which is 1 operation gestalt (operation gestalt 1) of this invention.

[0052] The gradation electrical-potential-difference generation circuit of this example 1 divides into eight equally between each gradation reference voltage of the gradation reference voltage (V0-V8) of nine values inputted from the internal power circuit 13 by the series resistance partial pressure circuit 1 as well as the gradation electrical-potential-difference generation circuit shown in said drawing 12 , and generates the gradation electrical potential difference for 64 gradation.

[0053] Here, it writes Vn [the gradation reference voltage Vn of the gradation reference voltage (V0-V8) of nine values and the electrical-potential-difference difference of gradation reference voltage Vn-1 (n=1-8)] (n-1), and it writes Rn [the gradation reference voltage Vn of the series resistance partial pressure circuit 1 and the combined-resistance value between the gradation criteria impression terminals of gradation reference voltage Vn-1 (n=1-8)].

[0054] the gradation electrical-potential-difference generation circuit of this operation gestalt 1 --

R8:R7:R6:R5:R4:R3:R2:R1=V8(7):V7(6):V6(5):V5 -- (4):V4(3):V3(2):V2(1): -

- it is V1 (0).
[0055] Therefore, the flowing current the series resistance partial pressure circuit 1 It becomes a fixed current value (Vn (n-1)/Rn = fixed current value). In the gradation electrical-potential-difference generation circuit of this operation gestalt 1 The inflow of the current from other than the gradation reference voltage (V0 and V8) impression terminal of the series resistance partial pressure circuit 1 where the greatest gradation reference voltage and the minimum gradation reference voltage electrical potential difference are impressed, Most outflows are set to 0, it becomes possible to reduce the power consumption of a drain driver, and this becomes possible to reduce the power consumption of a liquid crystal display.
[0056] Drawing 2 is drawing showing the example which applied concrete resistance to the series resistance partial pressure circuit 1 shown in drawing 1 , and carried out this invention.
[0057] The resistance of each resistance given in drawing 2 is an example which is shown in drawing 3 and which doubled the gradation reference voltages V0-V8 with the electrical-potential-difference permeability curve at the time of using the liquid crystal with which permeability is set to about 0 by 3V. V0' given in drawing 3 - V8' support the reference voltages V0-V8 of drawing 2 .
[0058] In the concrete example shown in drawing 2 , each current which flows to the resistance R1-R8 between each gradation reference voltage terminal is set to 1.3mA, and the power which a current does not flow for the terminal which impresses gradation reference voltages other than V0 and V8, but is consumed in the series resistance partial pressure circuit 1 originates in a 1.3mA current, and becomes the lowest.
[0059] Moreover, in the example shown in drawing 2 , the gradation electrical potential difference of V62 and V63 is set up highly, in order to give a black indication blacker and to raise contrast, the value of R88 and R87 is higher than the resistance of the other resistance R81-R86, and the items of the resistance R8 of the side near the terminal of a maximum voltage V8 are set up.
[0060] In the example similarly shown in drawing 2 , the gradation electrical potential difference of V00 and V01 is set up low, in order to give a white indication whiter and to raise contrast, the value of R11 and R12 is higher than the resistance of the other resistance R13-R17, and the items of the resistance R1 of the side near the terminal of the minimum electrical potential difference V0 are set up.
[0061] In addition, since the electrical potential difference which joins an actual liquid crystal layer (not shown) shows, V0' given in

drawing 3 - V8' have been shifted a changed part (0.8V) compared with the reference voltages V0-V8 of drawing 2 .

[0062] As a reason which the electrical potential difference which joins an actual liquid crystal layer shifts compared with the reference voltages V0-V8 of drawing 2 , the dive by the pixel electrode ITO of a gate voltage waveform can be considered. A gate voltage waveform is Gate with the drive approach which parasitic capacitance Cgs is between Gate G and the pixel electrode ITO as shown in an actual pixel at drawing 9 , and is shown in drawing 10 . From On to Gate If it changes to Off, since the pulse accompanying the change is impressed to the pixel electrode ITO through Cgs, the shift of an electrical potential difference which joins a liquid crystal layer will take place.

[0063] Therefore, to set up the gradation reference voltages V0-V8 of a power circuit 13, it is necessary to take into consideration the shift of an electrical potential difference which joins a liquid crystal layer beforehand.

[0064] In addition, the example shown in drawing 2 and drawing 3 shows the case where the electrical potential difference impressed to liquid crystal is negative polarity, and shows the case where a shifted part of an electrical potential difference is added to gradation reference voltage. However, since the value which lengthened a shifted part of an electrical potential difference from gradation reference voltage becomes the electrical potential difference impressed to an actual liquid crystal layer when the electrical potential difference impressed to liquid crystal is straight polarity, the gradation reference voltage generation circuit shown in drawing 13 is [2 class] necessary [of straight polarity and negative polarity].

[0065] The gradation electrical-potential-difference generation circuit in the drain driver 11 has two kinds of series resistance partial pressure circuits, straight polarity and negative polarity, 1 similarly, a polar signal is embraced, and it is change ******.

[0066] In addition, although the resistance between each gradation reference voltage impression terminal of the series resistance partial pressure circuit 1 is made into the resistance which is proportional to the potential difference between each gradation reference voltage completely in the gradation reference voltage generation circuit of this operation gestalt 1, even if it is not proportional completely, it has the same effectiveness.

[0067] That is, if dispersion in the value is within the limits of specification even if the value of Vn (n-1)/Rn is not completely in agreement, generating of excessive power consumption can be suppressed

compared with a specific thing out of range.
[0068] The series resistance partial pressure circuit 1 is made inside a semiconductor integrated circuit. There is dispersion in resistance generally made in a semiconductor integrated circuit, and when the diffused resistor of a semi-conductor is used for resistance, resistance produces **20% of dispersion. In addition, although it is also possible to sort out the done semiconductor integrated circuit and to make resistance into **10% of dispersion, since the yield of a semiconductor integrated circuit falls, the cost of the drain driver 11 becomes high. Therefore, it is not practical, although it is a liquid crystal display using the series resistance partial pressure circuit 1 shown in drawing 1 and it is ideal to make the value of Vn (n-1)/Rn completely in agreement.
[0069] Considering that the resistance R3 which affects a gradation display most differs in the example shown in drawing 2 **20%, **0.3mA (**23%) fluctuation of the current which flows to the value, R3 [i.e.,], of Vn (n-1)/Rn is carried out. Since R4 is the same resistance as R3, **0.3mA also of currents which flow to R4 is also changed. Considering the case where the difference of the current value which flows to R3 and R4 becomes the largest, a **0.6mA current flows for a terminal V3, and the power consumption of the series resistance partial pressure circuit 1 and a power circuit 13 increases.
[0070] However, since the current which flows to V1-V7 can be suppressed within the limits of **0.6mA if this operation gestalt is applied even if **20% of dispersion is in the resistance of the series resistance partial pressure circuit 1, the power consumption of the drain driver 11 and a power circuit 13 can be stopped low, and the cost of the drain driver 11 is highly practical.
[0071] If dispersion in the series resistance partial pressure circuit 1 is made **10% in the example furthermore shown in drawing 2 , the current which flows to R3 and R4 can be suppressed to **0.2mA (**15%) fluctuation. Therefore, considering the case where the difference of the current value which flows to R3 and R4 is max, a **0.4mA current can flow for a terminal V3, the increment in the power consumption of the series resistance partial pressure circuit 1 and a power circuit 13 can be made still smaller, and it is the most desirable.
[0072] In addition, when the power circuit 13 of a configuration of that it is shown in drawing 13 since the current which flows with this operation gestalt to the output terminal of V1-V7 of a power circuit can be suppressed low is used, the buffer circuits OP1-OP7 which output V1-V7 may have a high output impedance compared with the buffer circuits

OP0-OP8 which output V0 and V8, can use a cheap thing, and can lower the cost of a power circuit 13.
[0073] Furthermore, in this operation gestalt, except for buffer circuits OP1-OP7, the output of V1-V7 is possible also for obtaining from a direct-current-resistance partial pressure circuit, and can lower the cost of a power circuit 13 further.
[0074] Moreover, according to this operation gestalt, since the electrical-potential-difference difference is small, as for the gradation reference voltage difference V4 (3) which displays halftone as shown in drawing 1 , and V5 (4), the resistance R5 and R4 between the gradation reference voltage impression terminals of the series resistance partial pressure circuit 1 also becomes small.
[0075] When it sees in the concrete example shown in drawing 2 , namely, the gradation reference voltage difference V3 (2), Although V4 (3), V5 (4), and V6 (5) are lower than V1 (0), V2 (1), V7 (6), and V8 (7), since the value of R3-R6 is lower than the value of R1, R2, R7, and R8 enough It becomes possible to pass sufficient current for the output line of the gradation electrical potential difference (V15-V47) outputted from the resistance partial pressure circuit between V2 - V6.
[0076] Even if the number of the drain wire Dn which outputs the same gradation electrical potential difference increases by this, the voltage variation of the gradation electrical potential difference which a gradation electrical-potential-difference generation circuit outputs becomes small, and it becomes possible to suppress that a difference occurs in the brightness between pixels from which the drain driver 11 differs.
[0077] Therefore, ** which uses the gradation electrical-potential-difference generation circuit of this operation gestalt 1 enables it to constitute the liquid crystal display of a low power from high definition.
[0078] [Operation gestalt 2] Drawing 4 and drawing 5 are drawings showing the gradation electrical-potential-difference generation circuit of the drain driver of the liquid crystal display which are other operation gestalten (operation gestalt 2) of this invention.
[0079] The electrical-potential-difference permeability property generally shown in drawing 14 changes with ingredients of a liquid crystal layer.
[0080] Therefore, since the gradation reference voltage of a power circuit 13 is set up according to the electrical-potential-difference transmission property of a liquid crystal layer and the gradation electrical-potential-difference generation circuit in the drain driver

11 must also be set up according to an electrical-potential-difference transmission property, there is no versatility of the drain driver 11, the drain driver 11 of dedication must be used for every liquid crystal display panel, and there is a problem to which the cost of a liquid crystal display becomes high.

[0081] This operation gestalt 2 is an operation gestalt which made said operation gestalt 1 more concrete, and is an operation gestalt which enabled modification of the set point of the gradation electrical potential difference of the gradation electrical-potential-difference generation circuit of the drain driver 11 easily according to the liquid crystal display panel.

[0082] In the gradation reference voltage generation circuit of this operation gestalt 2, as a semi-conductor manufacture phase is shown in drawing 4 , the gradation reference voltage impression terminal of each gradation reference voltage (V1-V7) is connected to some points (A, B, C) of the series resistance partial pressure circuit 1 through a fuse 32.

[0083] In this case, each point of A, B, and C is chosen so that it may become the partial pressure value which may actually be used.

[0084] If predetermined gradation reference voltage is impressed as each gradation reference voltage (V0-V8) when actually using the gradation reference voltage generation circuit of this operation gestalt 2, a current will not flow at the fuse 32 connected at the place of the resistance proportional to the electrical-potential-difference difference of each gradation reference voltage, and a fuse 32 will not be melted.

[0085] However, a current flows at the other fuse 32, a fuse 32 is melted, and, thereby, the resistance between each gradation reference voltage impression terminal of the series resistance partial pressure circuit 1 turns into resistance proportional to the electrical-potential-difference difference of each gradation reference voltage.

[0086] Moreover, as shown in drawing 5 , each gradation voltage-output terminal 4 is similarly connected to some points (D, E, F) of the series resistance partial pressure circuit 1 through a fuse 2 at the side to which the output switch 3 of the series resistance partial pressure circuit 1 is connected.

[0087] After choosing the predetermined gradation V62, for example, gradation, based on the data for a display, a predetermined electrical potential difference is impressed to the gradation reference voltage impression terminal and the gradation voltage-output terminal 4 of the gradation reference voltages V8 and V7.

[0088] At this time, the electrical potential difference (0.8xV8(7))

corresponding to the resistance of the point that the fuse 2 not to melt is connected, for example, the point of E, is impressed to the gradation voltage-output terminal 4.

[0089] Thus, in the gradation electrical-potential-difference generation circuit of this operation gestalt 2, when melting the near fuse 2 to which the output switch 3 is connected, only the electrical-potential-difference difference of each gradation reference voltage is made into the value corresponding to the time of real use, and makes an absolute value an electrical potential difference higher than the time of real use.

[0090] Thereby, in the gradation electrical-potential-difference generation circuit of this operation gestalt 2, the current by which a fuse 2 is not melted at the time of real use can be passed.

[0091] As explained above, with this operation gestalt 2, versatility can be given to the drain driver 11 and it becomes possible like said operation gestalt 1 to realize easily the liquid crystal display which is a low power in high definition corresponding to the property of various liquid crystal display panels.

[0092] [Operation gestalt 3] Drawing 6 is drawing showing the gradation electrical-potential-difference generation circuit of the drain driver of the liquid crystal display which are other operation gestalten (operation gestalt 3) of this invention.

[0093] This operation gestalt 3 is also an operation gestalt which made said operation gestalt 1 more concrete, and is an operation gestalt whose modification of the set point of the gradation electrical potential difference of the gradation electrical-potential-difference generation circuit of the drain driver 11 was easily enabled according to the liquid crystal display panel.

[0094] The gradation electrical-potential-difference generation circuit of this operation gestalt 3 establishes how many kinds of two or more of those series resistance circuits (101,102,103) between the gradation reference voltage impression terminals of each gradation reference voltage (V0-V8) of the series resistance partial pressure circuit 1, and chooses the series resistance circuit (101,102,103) which serves as resistance ratio near the ratio of the electrical-potential-difference difference of each gradation reference voltage at the time of real use with a change signal.

[0095] Moreover, a changeover switch 5 is changed with a change signal, and it is made to output the gradation electrical potential difference from each series resistance circuit (101,102,103) to each gradation voltage-output terminal 4 similarly.

[0096] At this time, a change signal is supplied to each drain driver 11 from the input terminal of dedication of the register in a display control 10, EPROM, or the interface connector linked to a computer etc.
[0097] The series resistance partial pressure circuit which has the resistance ratio near the ratio of the electrical-potential-difference difference of each gradation reference voltage at the time of real use by this is easily realizable, and versatility can be given to the drain driver 11 and it becomes possible to realize easily the liquid crystal display which is a low power by high definition like said operation gestalt 1 corresponding to the property of various liquid crystal display panels also in the gradation electrical-potential-difference generation circuit of this operation gestalt 3.
[0098] [Operation gestalt 4] Drawing 7 is drawing showing the gradation electrical-potential-difference generation circuit of the drain driver of the liquid crystal display which are other operation gestalten (operation gestalt 4) of this invention.
[0099] This operation gestalt 4 is also an operation gestalt which made said operation gestalt 1 more concrete, and is an operation gestalt whose modification of the set point of the gradation electrical potential difference of the gradation electrical-potential-difference generation circuit of the drain driver 11 was easily enabled according to the liquid crystal display panel.
[0100] How many kinds of two or more of those series resistance circuits (101,102,103) are established between the gradation reference voltage impression terminals of each gradation reference voltage (V0-V8) of the series resistance partial pressure circuit 1, and the series resistance circuit (101,102,103) used as the resistance ratio near the ratio of the electrical-potential-difference difference of each gradation reference voltage is chosen in the gradation electrical-potential-difference generation circuit of this operation gestalt 4 as well as said operation gestalt 3 by modification of chisels, such as a metal wiring layer in a semi-conductor production process.
[0101] Moreover, similarly, it changes by modification of chisels, such as a metal wiring layer in a semi-conductor production process, a means 6 is changed, and it is made to output the gradation electrical potential difference from each series resistance circuit (101,102,103) to each gradation voltage-output terminal 4.
[0102] The series resistance partial pressure circuit which has the resistance ratio near the ratio of the electrical-potential-difference difference of each gradation reference voltage at the time of real use by this is easily realizable, and versatility can be given to the drain

driver 11 and it becomes possible to realize easily the liquid crystal display which is a low power by high definition like said operation gestalt 1 corresponding to the property of various liquid crystal display panels also in the gradation electrical-potential-difference generation circuit of this operation gestalt 4.

[0103] In addition, although said each operation gestalt explained the case where this invention was applied to a liquid crystal display, it is not limited to this and it cannot be overemphasized that this invention is applicable to all liquid crystal displays, such as a liquid crystal display module.

[0104] As mentioned above, although this invention was concretely explained based on the operation gestalt, it cannot be overemphasized that it can change variously in the range which this invention is not limited to said operation gestalt, and does not deviate from the summary.

[0105]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.

[0106] (1) In the gradation electrical-potential-difference generation circuit of the liquid crystal display which generates the multi-tone gradation electrical potential difference impressed to a liquid crystal layer according to this invention The resistance between each gradation reference voltage impression terminal of the series resistance partial pressure circuit 1 is proportional to the electrical-potential-difference difference between each gradation reference voltage. Among the gradation reference voltage impression terminals of a series resistance partial pressure circuit Most of the inflow of the current from other than the gradation reference voltage impression terminal with which the greatest gradation reference voltage and the minimum gradation reference voltage electrical potential difference are impressed, and an outflow is set to 0, it becomes possible to reduce the power consumption of drain DOREIBA, and this becomes possible to reduce the power consumption of a liquid crystal display.

[0107] (2) According to this invention, in the part of the halftone display with a large change of the permeability of the liquid crystal layer to applied voltage, since the resistance between gradation reference voltage impression terminals is small, even if the number of the drain signal line which outputs the same gradation electrical potential difference increases, the voltage variation of the gradation electrical potential difference of a gradation reference voltage generation circuit becomes possible [becoming small and suppressing

generating of the brightness difference of the display screen between different drain drivers 11].

[Translation done.]

* NOTICES *

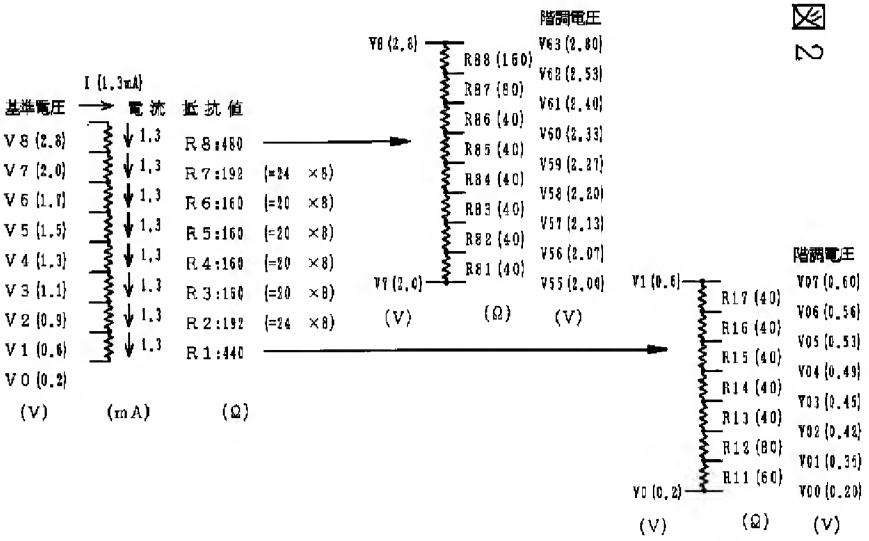
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the gradation electrical-potential-difference generation circuit of drain DOREIBA of the liquid crystal display which is 1 operation gestalt (operation gestalt 1) of this invention.
[Drawing 2] It is drawing which applied concrete resistance and a gradation reference voltage level to the gradation electrical-potential-difference generation circuit of drain DOREIBA of the liquid crystal display which is 1 operation gestalt (operation gestalt 1) of this invention.
[Drawing 3] It is drawing showing the relation between the gradation reference voltage shown in drawing 2 , and the permeability of a liquid crystal display component.
[Drawing 4] It is drawing showing the gradation electrical-potential-difference generation circuit of drain DOREIBA of the liquid crystal display which are other operation gestalten (operation gestalt 2) of this invention.
[Drawing 5] It is drawing showing the gradation electrical-potential-difference generation circuit of drain DOREIBA of the liquid crystal display which are other operation gestalten (operation gestalt 2) of this invention.
[Drawing 6] It is drawing showing the gradation electrical-potential-difference generation circuit of drain DOREIBA of the liquid crystal display which are other operation gestalten (operation gestalt 3) of

this invention.
[Drawing 7] It is drawing showing the gradation electrical-potential-difference generation circuit of drain DOREIBA of the liquid crystal display which are other operation gestalten (operation gestalt 4) of this invention.
[Drawing 8] It is the block diagram showing the outline configuration of a TFT-liquid-crystal indicating equipment.
[Drawing 9] It is drawing showing the equal circuit of the pixel of a TFT-liquid-crystal display.
[Drawing 10] It is drawing showing the timing relationship of the electrical potential difference impressed to the pixel of a TFT-liquid-crystal display.
[Drawing 11] It is the block diagram showing the outline configuration of a drain driver.
[Drawing 12] It is drawing showing the gradation electrical-potential-difference generation circuit of the conventional drain driver 11.
[Drawing 13] It is the circuit diagram of the gradation reference voltage generation section of a power circuit.
[Drawing 14] It is drawing which was shown in drawing 11 and in which showing the relation between gradation reference voltage and the permeability of a liquid crystal display component.
[Description of Notations]
TFT-LCD [-- A switch, 4 / -- A gradation voltage-output terminal, 5 / -- 6 A changeover switch, 7 / -- A change means, 10 / -- A display control, 11 / -- A drain driver, 12 / -- A gate driver, 13 / -- A power circuit, 101,102,103 / -- Series resistance circuit.] -- A TFT-liquid-crystal display panel, 1 -- 2 A series resistance partial pressure circuit, 32 -- A fuse, 3

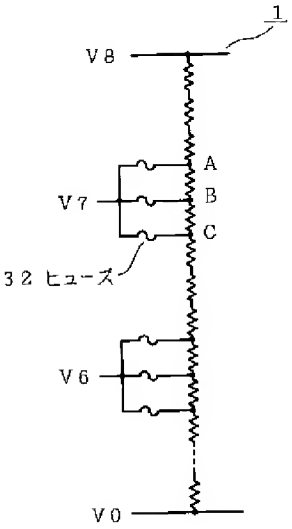
DRAWINGS

[Drawing 2]



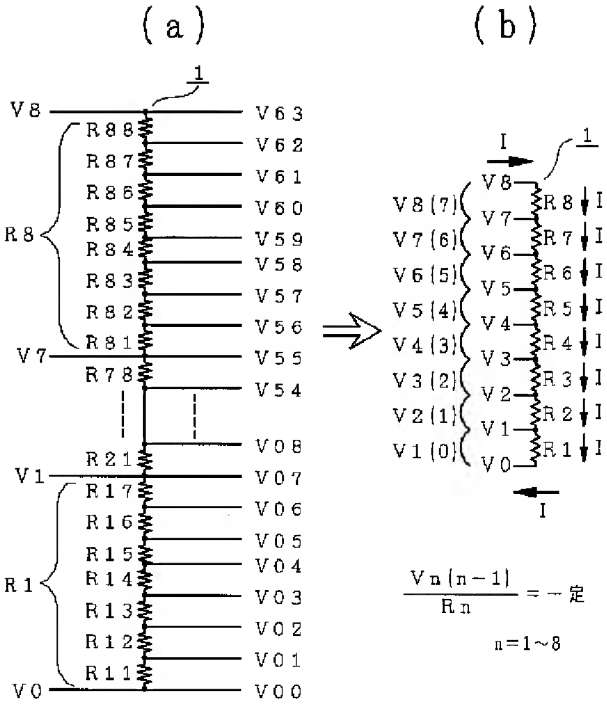
[Drawing 4]

図4



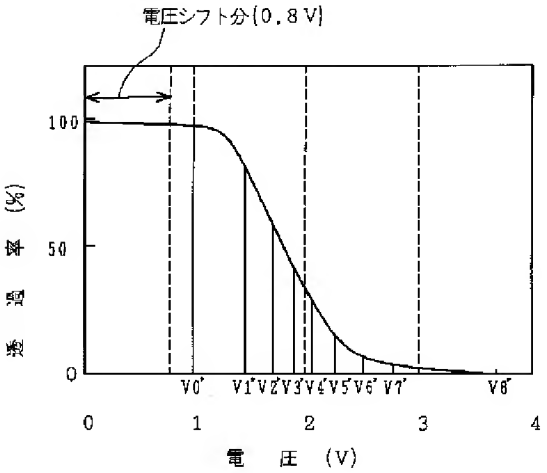
[Drawing 1]

図1



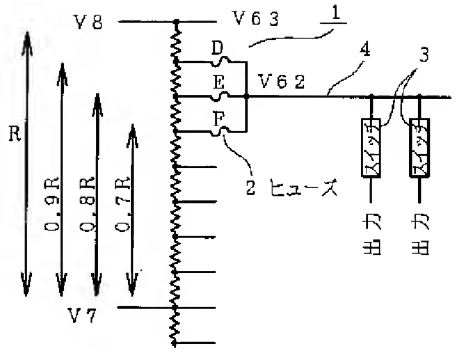
[Drawing 3]

図3



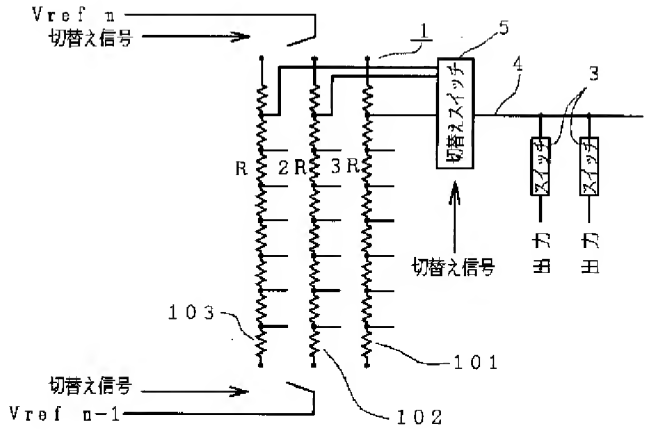
[Drawing 5]

図5



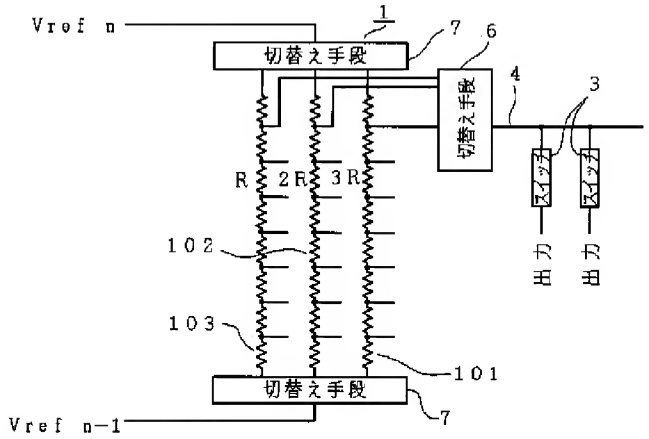
[Drawing 6]

図6



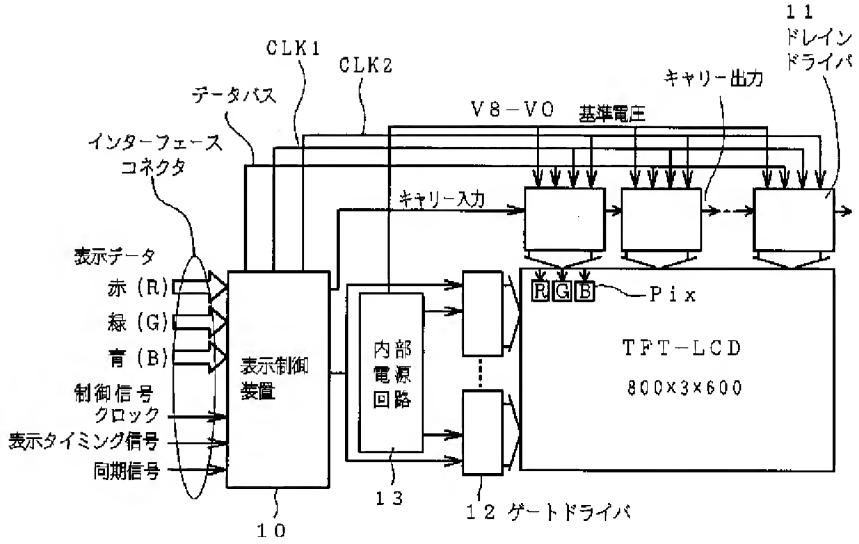
[Drawing 7]

図7



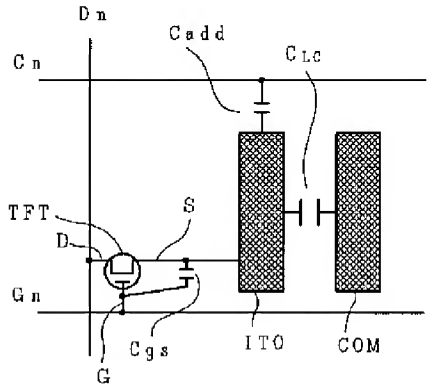
[Drawing 8]

図8



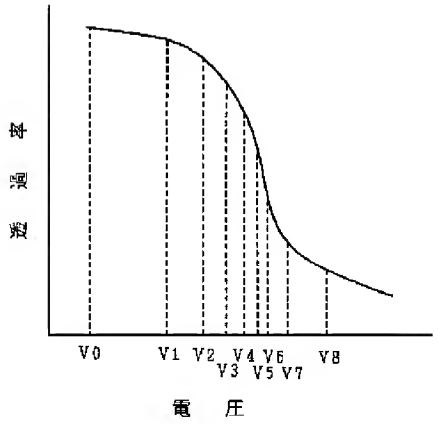
[Drawing 9]

図9



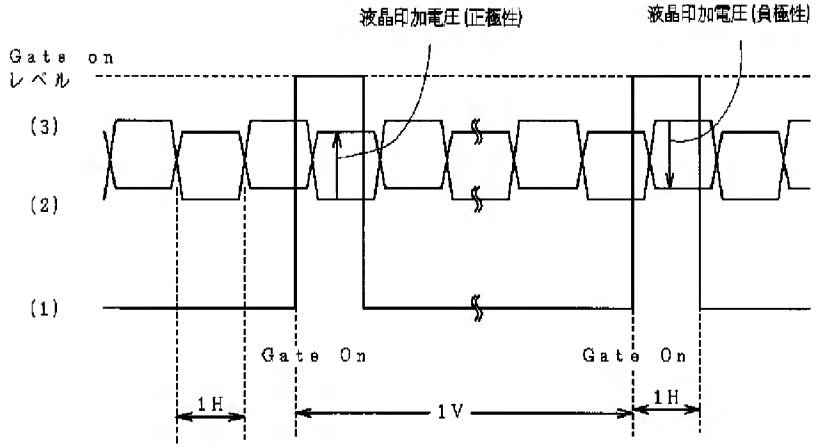
[Drawing 14]

図１４



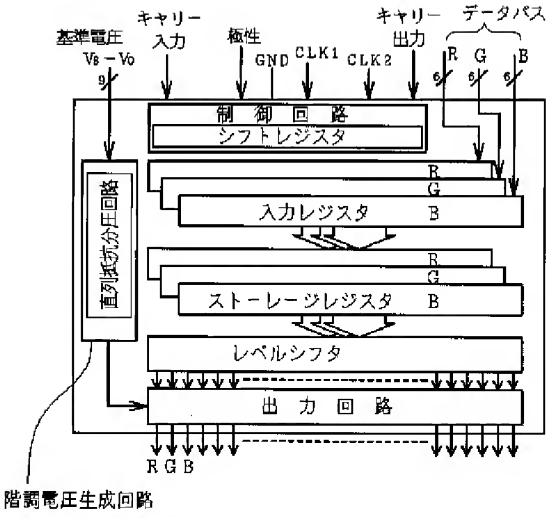
[Drawing 10]

図１０



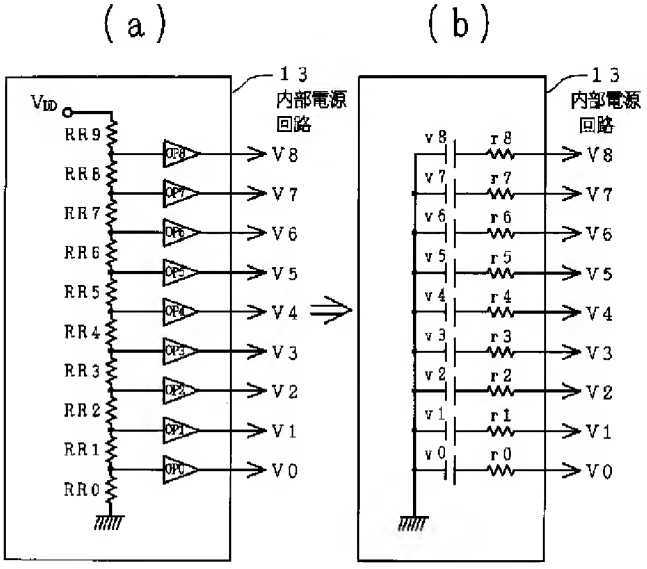
[Drawing 11]

図１１



[Drawing 13]

図１３



[Drawing 12]

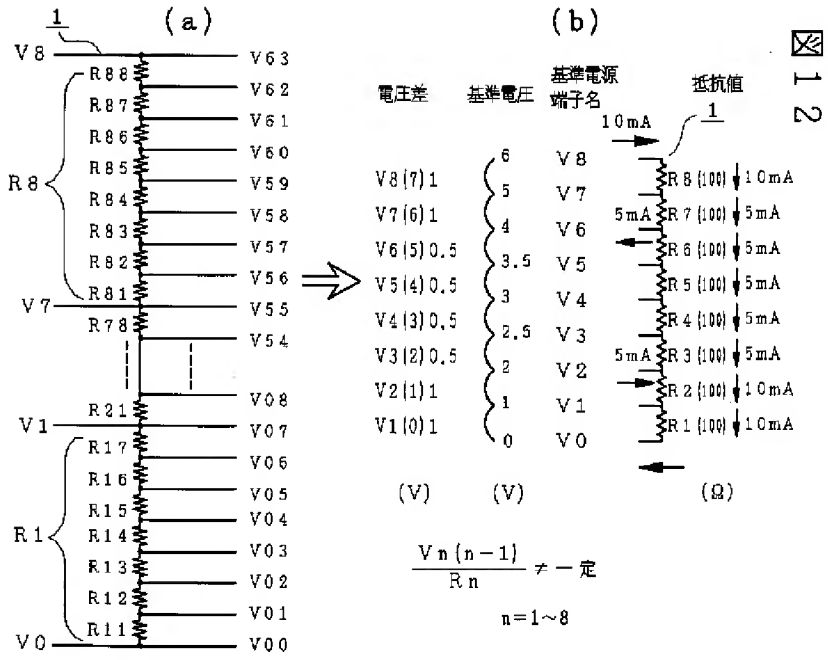


図12

[Translation done.]

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最終頁に続く

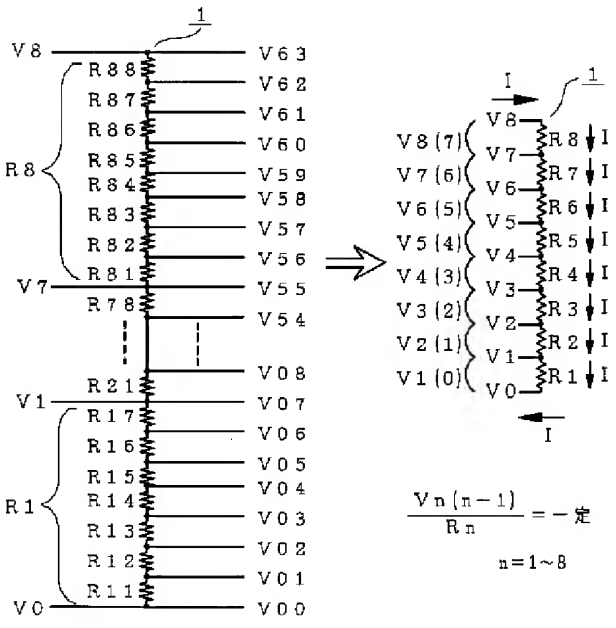
(54)【発明の名称】　液晶表示装置

(57)【要約】

【課題】　低消費電力と高画質表示を可能とする液晶表示装置の階調電圧生成回路を提供すること。

【解決手段】　複数の階調基準電圧の各階調基準電圧間を直列抵抗分圧回路により分圧して液晶層に印加する多階調の階調電圧を生成する液晶表示装置であって、前記直列抵抗分圧回路の各階調基準電圧を印加する端子間の抵抗値を、各階調基準電圧間の電位差にほぼ比例した抵抗値とする。

図１



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【特許請求の範囲】

【請求項１】　薄膜トランジスタと該薄膜トランジスタのソースに電気的に接続された画素電極とを有する画素が複数配置された液晶表示パネルと、上記薄膜トランジスタのドレインに、複数の電位の階調電圧から選択した、電圧を出力するドレインドライバと、上記ドレインドライバに複数の電位の階調基準電圧を出力する電源回路と、上記薄膜トランジスタのゲートに、上記画素を選択する、電圧を出力するゲートドライバとを有する液晶表示装置であって、

上記ドレインドライバは階調電圧生成回路を有し、上記階調電圧生成回路は、上記複数の階調基準電圧の電位間を、抵抗を直列に接続した分圧回路により複数の電位に分圧し、上記複数の電位の階調電圧を生成し、

上記分圧回路の各階調基準電圧の電位間の抵抗値を、各階調基準電圧間の電位差にほぼ比例した抵抗値に設定したことを特徴とする液晶表示装置。

【請求項２】　上記分圧回路の各階調基準電圧の電位間の抵抗値を、各階調基準電圧間の電位差にほぼ比例した抵抗値に変更するための切替手段を具備することを特徴とする請求項１に記載された液晶表示装置。

【請求項３】　上記分圧回路の各階調基準電圧の電位間に複数の直列抵抗回路を設け、前記複数の直列抵抗回路の中から、各階調基準電圧間の電位差にほぼ比例した抵抗値となる直列抵抗回路を選択するための選択手段を具備することを特徴とする請求項１に記載された液晶表示装置。

【請求項４】　薄膜トランジスタと該薄膜トランジスタのソースに電気的に接続された画素電極とを有する画素が複数配置された液晶表示パネルと、上記薄膜トランジスタのドレインに、複数の電位の階調電圧から選択した、電圧を出力するドレインドライバと、上記ドレインドライバに複数の電位の階調基準電圧を出力する電源回路と、上記薄膜トランジスタのゲートに、上記画素を選択する、電圧を出力するゲートドライバとを有する液晶表示装置であって、

上記ドレインドライバは階調電圧生成回路を有し、上記階調電圧生成回路は、上記複数の階調基準電圧の電位間を、抵抗を直列に接続した分圧回路により複数の電位に分圧し、上記複数の電位の階調電圧を生成し、

上記一つの階調基準電圧Ｖｎと他の階調基準電圧Ｖｎ－１との電位差をＶｎ（ｎ－１）とし、上記階調基準電圧ＶｎとＶｎ－１の上記分圧回路の印加端子間の合成抵抗値をＲｎとすると、全てのＲｎに対してＶｎ（ｎ－１）／Ｒｎの値が特定の変動の範囲内で一致するように上記分圧回路の各抵抗の値を設定したことを特徴とする液晶表示装置。

【請求項５】　上記全てのＲｎに対して上記Ｖｎ（ｎ－１）／Ｒｎの値が±２３％の変動の範囲内で一致するように上記分圧回路の各抵抗の値を設定したことを特徴とする請求項４に記載された液晶表示装置。

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【請求項６】　上記全てのＲｎに対して上記Ｖｎ（ｎ－１）／Ｒｎの値が±１５％の変動の範囲内で一致するように上記分圧回路の各抵抗の値を設定したことを特徴とする請求項４に記載された液晶表示装置。

【請求項７】　上記全てのＲｎに対して上記Ｖｎ（ｎ－１）／Ｒｎの値が完全に一致するように上記分圧回路の各抵抗の値を設定したことを特徴とする請求項４に記載された液晶表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、パーソナルコンピュータ、ワークステーション等に用いる液晶表示装置に関し、特に、多階調の表示が可能な液晶表示装置の階調電圧生成回路に関する。

【０００２】

【従来の技術】多色表示、例えば、６４階調の多色表示が可能なＴＦＴ液晶表示装置の一例が下記文献Ｉに記載されている。

【０００３】Ｉ　『Ｌｏｗ－Ｐｏｗｅｒ　６－ｂｉｔ　Ｃｏｌｕｍｎ　Ｄｒｉｖｅｒｆｏｒ　ＡＭＬＣＤｓ』（１９９４年６月発行　ＳＩＤ　９４　ＤＩＪＥＳＴ　Ｐ．３５１－３５４）。

【０００４】図８は、前記文献Ｉに記載されているＴＦＴ液晶表示装置の概略構成を示すブロック図である。

【０００５】図８において、液晶表示パネル（ＴＦＴ－ＬＣＤ）は、８００×３×６００画素Ｐｉｘから構成される。

【０００６】ＴＦＴ液晶表示パネルの画素Ｐｉｘの等価回路を図９に示す。

【０００７】ＩＴＯは画素電極、ＣＯＭは対向電極で、ＩＴＯとＣＯＭと液晶層で液晶表示素子（図示せず）が形成される。

【０００８】液晶表示素子は等価回路で示すと静電容量ＣＬＣで表せる。

【０００９】液晶表示素子は図１４に示すようにＩＴＯとＣＯＭの間に印加する電圧により光の透過率が変化するので、画素電極ＩＴＯに、ＣＯＭに印加する電圧を基準として複数の表示階調毎に電圧が決められた、階調電圧を印加することにより多階調表示ができる。

【００１０】Ｄｎはドレイン線あるいは映像信号線であり、階調電圧はドレインドライバ１１から複数のドレイン線Ｄｎに印加される。

【００１１】ＴＦＴは薄膜トランジスタであり、ＩＴＯに電気的に接続されるソースＳ、Ｄｎに電気的に接続されるドレインＤ及びゲートＧを有し、ゲートＧに加える電圧によりＤｎ、ＩＴＯ間の電気的導通、非導通を制御する。

【００１２】Ｇｎはゲート線あるいは走査線であり、Ｇｎは対応する画素ＰｉｘのＴＦＴのゲートＧに接続され

ているので、Ｇｎにより階調電圧を印加する画素電極ＩＴＯを選択することが出来る。

【００１３】Ｃａｄｄは保持容量、Ｃｎは容量線で、ＣａｄｄはＩＴＯに印加された階調電圧を、次に階調電圧がＩＴＯに印加される迄の間、保持することが出来る。

【００１４】図１０は図９に示す画素に印加される電圧波形のタイミングを示す図である。

【００１５】同図で（１）はゲート線Ｇｎの波形、（２）は対向電極ＣＯＭ及び容量線Ｃｎの波形、（３）はドレイン線Ｄｎの波形を示す。画素電極ＩＴＯに階調電圧を印加する時はゲート電圧波形（１）が　Ｇａｔｅ　Ｏｎ　レベルとなりＴＦＴのソース、ドレイン間が導通する。ドレイン電圧波形（３）と対向電極電圧波形（２）は位相が反転した形になっており、ドレイン電圧波形（３）と対向電極電圧波形（２）の差の電圧が液晶表示素子ＣＬＣに印加される。液晶表示素子ＣＬＣに印加される電圧は、正極性で印加されるタイミングと負極性で印加されるタイミングが交互に現れるように、ゲート電圧波形（１）、対向電極電圧波形（２）、ドレイン電圧波形（３）を設定しているので、液晶表示素子ＣＬＣには直流成分が印加されず、ＴＦＴ液晶表示パネルの寿命の低下、画像の焼き付き及び残像の問題が無い。

【００１６】ＴＦＴを用いた液晶表示装置の特徴は、ＴＦＴというスイッチング素子を介して画素電極ＩＴＯに階調電圧を印加する為各画素Ｐｉｘ間のクロストークが無く、単純マトリックス形液晶表示装置のようにクロストークを防止する為の特殊な駆動方法を用いる必要が無く、多階調表示が可能なことにある。

【００１７】また図８に示すように、液晶表示パネル（ＴＦＴ－ＬＣＤ）の一方の側にドレインドライバ１１が配置され、このドレインドライバ１１を薄膜トランジスタ（ＴＦＴ）のドレイン線に接続し、薄膜トランジスタ（ＴＦＴ）に液晶を駆動するための電圧を供給する。

【００１８】また、液晶表示パネル（ＴＦＴ－ＬＣＤ）の側面にはゲートドライバ１２が配置され、薄膜トランジスタ（ＴＦＴ）のゲート線に接続し、１水平動作時間（１Ｈ）薄膜トランジスタ（ＴＦＴ）のゲートＧにＧａｔｅ　Ｏｎ電圧を供給する。

【００１９】表示制御装置１０は、インターフェースコネクタから、本体コンピュータからの表示用データと表示制御信号を受け取り、これを基にドレインドライバ１１，ゲートドライバ１２を駆動する。

【００２０】ここで、本体コンピュータからの表示用データは、各色毎６ビットの１８ビットで構成されている。

【００２１】ドレインドライバ１１は、図１１に示すように、１個の階調電圧生成回路を有し、前記階調電圧生成回路は、内部電源回路１３から入力される９値の階調基準電圧（Ｖ０－Ｖ８）から６４階調分の階調電圧を生成する。

【００２２】また、ドレインドライバ１１は、シフトレジスタにより表示データラッチ用クロック信号ＣＬＫ１に同期して各色毎６ビットの表示用データを入力レジスタ内に出力本数分だけ取り込む。次に、出力タイミング制御用クロック信号ＣＬＫ２に応じて、入力レジスタ内の表示用データをストーレージレジスタに取り込み、出力回路は前記階調電圧生成回路で生成された６４階調分の階調電圧の中から、表示用データに対応する階調電圧を選択して各ドレイン線Ｄｎに出力する。

【００２３】ドレインドライバ１１の極性端子はドレイン線Ｄｎに出力する電圧の極性を制御する為に設けられ、キャリー入力、キャリー出力端子は液晶表示装置内の複数のドレインドライバ１１間の連携を取る為に設けられている。

【００２４】図１２は、前記図１１に示すドレインドライバ１１の階調電圧生成回路を示す図である。

【００２５】図１２の（ａ）に示すように、前記図１１に示すドレインドライバ１１の階調電圧生成回路は、内部電源回路１３から入力された９値の階調基準電圧（Ｖ０－Ｖ８）の各階調基準電圧間を、直列抵抗分圧回路１により８等分してＶ００～Ｖ６３の６４階調分の階調電圧を生成するものである。

【００２６】

【発明が解決しようとする課題】図１４に示すように、一般に液晶層に印加する電圧と透過率との関係は、リニアではなく、透過率の高いところ及び低いところでは、液晶層に印加する電圧に対する透過率の変化は少なく、その中間となるところで透過率の変化が大きい。

【００２７】このため、６４階調の多色表示が可能な液晶表示装置において、６４階調をリニアに表示するためには、ドレインドライバ１１の階調電圧生成回路に与える階調基準電圧値は、等間隔ではなく、中間調付近（Ｖ２～Ｖ６）で差が小さく、それ以外（Ｖ０～Ｖ２，Ｖ６～Ｖ８）で大きくしなければならない。

【００２８】ところが前記文献では、前記図１２に示すドレインドライバ１１の階調電圧生成回路の直列抵抗分圧回路１の抵抗値をどのように設定するかは詳しく言及していない。

【００２９】そのため、図１２の（ａ）に示す階調電圧生成回路の直列抵抗分圧回路１に、図１４に示す等間隔ではない階調基準電圧Ｖ０～Ｖ８を印加すると、階調基準電圧を供給する線に直流（ＤＣ）電流が流れ、消費電力が増大する問題があった。

【００３０】例えば図１２の（ｂ）は同図（ａ）を簡略化したものであるが、階調電圧生成回路において直列抵抗分圧回路１の各階調基準電圧印加端子間の抵抗値はそれぞれ１００Ωで一定の値にすると、階調基準電圧Ｖ０－Ｖ１間、Ｖ１－Ｖ２間、Ｖ６－Ｖ７間、Ｖ７－Ｖ８間の階調基準電圧差が、階調基準電圧Ｖ２－Ｖ３間、Ｖ３－Ｖ４間、Ｖ４－Ｖ５間、Ｖ５－Ｖ６間の階調基準電圧

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差の２倍となる。

【００３１】したがって、直列抵抗分圧回路１の階調基準電圧Ｖ６，Ｖ７の階調基準電圧を印加する端子間、および、階調基準電圧Ｖ１，Ｖ２の階調基準電圧を印加する端子間を流れる電流は、１０ｍＡ（１．０Ｖ／１００Ω＝１０ｍＡ）であるのに対して、直列抵抗分圧回路１の階調基準電圧Ｖ５，Ｖ６、および、階調基準電圧Ｖ２，Ｖ３の階調基準電圧を印加する端子間を流れる電流は、５ｍＡ（０．５Ｖ／１００Ω＝５ｍＡ）となる。

【００３２】そのため、電流値が不連続となる直列抵抗分圧回路１の階調基準電圧Ｖ６を印加する端子、および、階調基準電圧Ｖ２を印加する端子から電流が流入・流出し、階調電圧生成回路に流れる電流が多くなる為、ドレインドライバ１１の消費電力が増大するという問題があった。

【００３３】また階調基準電圧Ｖ１～Ｖ７を供給する線に電流が流入・流出すると電源回路１３の内部抵抗による消費電力の増加も問題であった。

【００３４】図１３は電源回路１３の階調基準電圧Ｖ０～Ｖ８の生成部を示す図である。

【００３５】同図（ａ）は階調基準電圧Ｖ０～Ｖ８の生成部を抵抗分圧回路で生成する例を示す。階調基準電圧Ｖ０～Ｖ８は抵抗ＲＲ０～ＲＲ９の値の比により設定され、抵抗ＲＲ０～ＲＲ９の分圧回路の出力は、バッファ回路ＯＰ０～ＯＰ９により、充分な電力に増幅されてドレインドライバ１１の直列抵抗分圧回路１に出力される。

【００３６】同図（ｂ）は同図（ａ）の等価回路を示す図である。電源回路１３は直流電圧源ｖ０～ｖ８と内部抵抗ｒ０～ｒ８で表すことが出来る。直流電圧源ｖ０～ｖ８は抵抗ＲＲ０～ＲＲ９の分圧回路の出力により決まり、内部抵抗ｒ０～ｒ８はバッファ回路ＯＰ０～ＯＰ９の出力インピーダンスにより決まると考えられる。

【００３７】仮に内部抵抗ｒ０～ｒ８を２０Ωにしたとすると、階調基準電圧Ｖ２の供給線に５ｍＡの電流が流れると０．５ｍＷの電力が余分に電源回路１３で消費されることになる。また内部抵抗ｒ２により０．２Ｖの電圧降下を生じるので、ドレインドライバ１１に出力する階調基準電圧Ｖ２も０．２Ｖ降下し、目的とする階調電圧を液晶表示パネルに出力出来ず、正しい表示階調が得られない問題も生じる。

【００３８】またドレインドライバ１１では、構成を簡単にし集積回路のチップサイズを小さくする目的で、図１１に示すように、階調電圧生成回路の出力をドレインドライバ１１が駆動する全てのドレイン線で共用する為、１つのドレインドライバ１１内で同一階調電圧を選択するドレイン信号線の本数が多くなると、階調基準電圧生成回路１の抵抗Ｒ１～Ｒ８に流れる電流が大きくなり、各階調電圧がドレインドライバ１１毎に変動し、特に、印加電圧に対する液晶層の透過率の変化が大きい中

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間調表示（Ｖ２～Ｖ６）の表示画面上では、ドレインドライバ１１が異なるドレイン線Ｄｎ，Ｄｎ＋１に対応する画素Ｐｉｘの境界で輝度差が発生し表示品質が低下するという問題点があった。

【００３９】すなわち図１２に示す例で見ると、階調基準電圧差Ｖ３（２），Ｖ４（３），Ｖ５（４），Ｖ６（５）はＶ１（０），Ｖ２（１），Ｖ７（６），Ｖ８（７）よりも低いが、Ｒ３～Ｒ６の値はＲ１，Ｒ２，Ｒ７，Ｒ８の値と同じなので、Ｖ２～Ｖ６間の抵抗分圧回路から出力される階調電圧（Ｖ１５～Ｖ４７）の出力線には充分な電流を流すことが困難になる。

【００４０】本発明は、前記従来技術の問題点を解決するためになされたものであり、本発明の目的は、液晶表示装置の階調電圧生成回路において、低消費電力と高画質表示を可能とする液晶表示装置を提供することにある。

【００４１】本発明の前記目的並びにその他の目的及び新規な特徴は、本明細書の記載及び添付図面によって明らかにする。

【００４２】

【課題を解決するための手段】本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、下記の通りである。

【００４３】（１）複数の階調基準電圧の各階調基準電圧間を直列抵抗分圧回路により分圧して液晶層に印加する多階調の階調電圧を生成する液晶表示装置であって、前記直列抵抗分圧回路の各階調基準電圧を印加する端子間の抵抗値を、各階調基準電圧間の電位差にほぼ比例した抵抗値としたことを特徴とする。

【００４４】（２）前記（１）の手段において、前記直列抵抗分圧回路の各階調基準電圧を印加する端子間の抵抗値を、各階調基準電圧間の電位差にほぼ比例した抵抗値に変更するための切替手段を具備することを特徴とする。

【００４５】（３）前記（１）の手段において、前記直列抵抗分圧回路の各階調基準電圧を印加端する子間に複数の直列抵抗回路を設け、前記複数の直列抵抗回路の中から、各階調基準電圧間の電位差にほぼ比例した抵抗値となる直列抵抗回路を選択するための選択手段を具備することを特徴とする。

【００４６】前記各手段によれば、液晶層に印加する多階調の階調電圧を生成する液晶表示装置の階調電圧生成回路において、直列抵抗分圧回路の各階調基準電圧印加端子間の抵抗値が、各階調基準電圧間の電圧差に比例しており、直列抵抗分圧回路の階調基準電圧印加端子のうちで、最大の階調基準電圧と最小の階調基準電圧電圧とが印加される階調基準電圧印加端子以外からの電流の流入、流出はほとんど０となり、ドレインドライバ１１及び電源回路１３の消費電力を低減することが可能となり、液晶表示装置全体の消費電力を低減することが出来

る。

【００４７】また、印加電圧に対する液晶層の透過率の変化が大きい中間調表示の部分では、階調基準電圧印加端子間の抵抗値を小さくするため、同一階調電圧を出力するドレイン信号線の本数が多くなっても、階調電圧生成回路の階調電圧の電圧変動が小さくなり、ドレインドライバ１１が異なる、画素Ｐｉｘ間の境界で輝度差が発生するのを抑えることが可能となり、液晶表示装置の表示特性が向上する。

【００４８】

【発明の実施の形態】以下、本発明を適用したＴＦＴ液晶表示装置の実施形態について図面を参照して詳細に説明する。

【００４９】なお、実施形態を説明するための全図において、同一機能を有するものは同一符号を付け、その繰り返しの説明は省略する。

【００５０】以下、本発明が適用されるＴＦＴ液晶表示装置構成は、前記図８に示すＴＦＴ液晶表示装置と同じであるので説明は省略する。

【００５１】〔実施形態１〕図１は、本発明の一実施形態（実施形態１）である液晶表示装置のドレインドライバ１１の階調電圧生成回路を示す図である。

【００５２】本実施例１の階調電圧生成回路は、前記図１２に示す階調電圧生成回路と同じく、内部電源回路１３から入力された９値の階調基準電圧（Ｖ０－Ｖ８）の各階調基準電圧間を、直列抵抗分圧回路１により８等分して６４階調分の階調電圧を生成するものである。

【００５３】ここで、９値の階調基準電圧（Ｖ０－Ｖ８）の階調基準電圧Ｖｎと階調基準電圧Ｖｎ－１（ｎ＝１～８）の電圧差をＶｎ（ｎ－１）と表記し、直列抵抗分圧回路１の階調基準電圧Ｖｎと階調基準電圧Ｖｎ－１（ｎ＝１～８）の階調基準印加端子間の合成抵抗値をＲｎと表記する。

【００５４】本実施形態１の階調電圧生成回路では、Ｒ８：Ｒ７：Ｒ６：Ｒ５：Ｒ４：Ｒ３：Ｒ２：Ｒ１＝Ｖ８（７）：Ｖ７（６）：Ｖ６（５）：Ｖ５（４）：Ｖ４（３）：Ｖ３（２）：Ｖ２（１）：Ｖ１（０）である。

【００５５】したがって、直列抵抗分圧回路１を流れる電流は、一定の電流値（Ｖｎ（ｎ－１）／Ｒｎ＝一定の電流値）となり、本実施形態１の階調電圧生成回路では、最大の階調基準電圧と最小の階調基準電圧電圧とが印加される直列抵抗分圧回路１の階調基準電圧（Ｖ０およびＶ８）印加端子以外からの電流の流入、流出はほとんど０となり、ドレインドライバの消費電力を低減することが可能となり、それにより、液晶表示装置の消費電力を低減することが可能となる。

【００５６】図２は図１に示す直列抵抗分圧回路１に具体的な抵抗値を当てはめて本発明を実施した例を示す図である。

【００５７】図２に記載の各抵抗の抵抗値は、図３に示す、３Ｖで透過率がほぼ０になる液晶を用いた場合の電圧透過率曲線に階調基準電圧Ｖ０～Ｖ８を合わせた例である。図３に記載のＶ０’～Ｖ８’は図２の基準電圧Ｖ０～Ｖ８に対応している。

【００５８】図２に示す具体的な実施例では各階調基準電圧端子間の抵抗Ｒ１～Ｒ８に流れる電流は何れも１．３ｍＡとなり、Ｖ０，Ｖ８以外の階調基準電圧を印加する端子には電流が流れず、直列抵抗分圧回路１で消費する電力は、１．３ｍＡの電流に起因するもののみで、最も低くなる。

【００５９】また図２に示す実施例においては、Ｖ６２，Ｖ６３の階調電圧を高く設定して黒の表示をより黒くしてコントラストを高める為に、最高電圧Ｖ８の端子に近い側の抵抗Ｒ８の内訳はＲ８８，Ｒ８７の値がその他の抵抗Ｒ８１～Ｒ８６の抵抗値よりも高く設定されている。

【００６０】同様に図２に示す実施例においては、Ｖ００，Ｖ０１の階調電圧を低く設定して白の表示をより白くしてコントラストを高める為に、最低電圧Ｖ０の端子に近い側の抵抗Ｒ１の内訳はＲ１１，Ｒ１２の値がその他の抵抗Ｒ１３～Ｒ１７の抵抗値よりも高く設定されている。

【００６１】なお図３に記載のＶ０’～Ｖ８’は、実際の液晶層（図示せず）に加わる電圧で示している為、図２の基準電圧Ｖ０～Ｖ８に比べ変動分（０．８Ｖ）だけシフトしている。

【００６２】実際の液晶層に加わる電圧が図２の基準電圧Ｖ０～Ｖ８に比べシフトする理由としてはゲート電圧波形の画素電極ＩＴＯへの飛込みが考えられる。実際の画素には図９に示すようにゲートＧ、画素電極ＩＴＯ間には寄生容量ＣｇｓがあＲ、図１０に示す駆動方法でゲート電圧波形がＧａｔｅ　ＯｎからＧａｔｅ　Ｏｆｆに変化すると、その変化に伴うパルスがＣｇｓを介して画素電極ＩＴＯに印加されるため液晶層に加わる電圧のシフトが起こる。

【００６３】従って電源回路１３の階調基準電圧Ｖ０～Ｖ８を設定する場合は予め液晶層に加わる電圧のシフトを考慮に入れる必要がある。

【００６４】なお、図２、図３に示す実施例は液晶に印加する電圧が負極性の場合を示したものであり、電圧のシフト分を階調基準電圧に加える場合を示している。しかし液晶に印加する電圧が正極性の場合は電圧のシフト分を階調基準電圧から引いた値が実際の液晶層に印加される電圧になる為、図１３に示す階調基準電圧生成回路は正極性と負極性の２種類必要になる。

【００６５】同様にドレインドライバ１１内の階調電圧生成回路も正極性と負極性の２種類の直列抵抗分圧回路１を有し、極性信号に応じて切替ている。

【００６６】なお、本実施形態１の階調基準電圧生成回路では、直列抵抗分圧回路１の各階調基準電圧印加端子

間の抵抗値を、各階調基準電圧間の電位差に完全に比例した抵抗値としているが、完全に比例していなくても、同様な効果を有する。

【００６７】すなわちＶｎ（ｎ－１）／Ｒｎの値が完全に一致していなくとも、その値のばらつきが特定の範囲内にあれば、特定の範囲外のものに比べ、余分な消費電力の発生を抑えることが出来る。

【００６８】直列抵抗分圧回路１は半導体集積回路の内部に作られる。一般に半導体集積回路内に作られる抵抗にはばらつきがあり、抵抗に半導体の拡散抵抗を用いた場合、抵抗値は±２０％のばらつきを生じる。なお出来上がった半導体集積回路を選別して抵抗値を±１０％のばらつきにすることも可能であるが、半導体集積回路の歩留が下がるのでドレインドライバ１１のコストが高くなる。従って図１に示した直列抵抗分圧回路１を用いる液晶表示装置で、Ｖｎ（ｎ－１）／Ｒｎの値を完全に一致させるのは理想的であるが、実用的ではない。

【００６９】図２に示す実施例で、最も階調表示に影響を与える、抵抗Ｒ３が±２０％ばらつくことを考えると、Ｖｎ（ｎ－１）／Ｒｎの値即ちＲ３に流れる電流は±０．３ｍＡ（±２３％）変動する。Ｒ４もＲ３と同じ抵抗値なのでＲ４に流れる電流も±０．３ｍＡ変動する。Ｒ３とＲ４に流れる電流値の差が最も大きくなった場合を考えると、端子Ｖ３には±０．６ｍＡの電流が流れ直列抵抗分圧回路１及び電源回路１３の消費電力が増加する。

【００７０】しかし直列抵抗分圧回路１の抵抗値に±２０％のばらつきがあっても、本実施形態を適用すればＶ１～Ｖ７に流れる電流を±０．６ｍＡの範囲内に抑えることが出来るので、ドレインドライバ１１及び電源回路１３の消費電力を低く抑えることが出来、ドレインドライバ１１のコストが高くなく実用的である。

【００７１】さらに図２に示す実施例で直列抵抗分圧回路１のばらつきを±１０％にすると、Ｒ３、Ｒ４に流れる電流は±０．２ｍＡ（±１５％）の変動に抑えることが出来る。従ってＲ３とＲ４に流れる電流値の差が最大の場合を考えると、端子Ｖ３には±０．４ｍＡの電流が流れ直列抵抗分圧回路１及び電源回路１３の消費電力の増加をさらに小さくすることが出来、最も好ましい。

【００７２】なお本実施形態では電源回路のＶ１～Ｖ７の出力端子に流れる電流は低く抑えることが出来る為、図１３に示す構成の電源回路１３を用いた場合には、Ｖ１～Ｖ７を出力するバッファ回路ＯＰ１～ＯＰ７はＶ０，Ｖ８を出力するバッファ回路ＯＰ０～ＯＰ８に比べ出力インピーダンスが高くても良く、安価なものが使用出来、電源回路１３のコストを下げることが出来る。

【００７３】さらに本実施形態においては、バッファ回路ＯＰ１～ＯＰ７を除いて、Ｖ１～Ｖ７の出力は直接抵抗分圧回路から得ることも可能であり、電源回路１３のコストを更に下げることが出来る。

【００７４】また本実施形態によれば、図１に示すように中間調を表示する階調基準電圧差Ｖ４（３）、Ｖ５（４）は、電圧差が小さいため、直列抵抗分圧回路１の階調基準電圧印加端子間の抵抗値Ｒ５、Ｒ４も小さくなる。

【００７５】すなわち図２に示す具体的実施例で見ると、階調基準電圧差Ｖ３（２），Ｖ４（３），Ｖ５（４），Ｖ６（５）はＶ１（０），Ｖ２（１），Ｖ７（６），Ｖ８（７）よりも低いが、Ｒ３～Ｒ６の値はＲ１，Ｒ２，Ｒ７，Ｒ８の値よりも充分低いので、Ｖ２～Ｖ６間の抵抗分圧回路から出力される階調電圧（Ｖ１５～Ｖ４７）の出力線には充分な電流を流すことが可能になる。

【００７６】これにより、同一階調電圧を出力するドレイン線Ｄｎの本数が多くなっても、階調電圧生成回路の出力する階調電圧の電圧変動が小さくなり、ドレインドライバ１１が異なる、画素間の輝度に差が発生するのを抑えることが可能となる。

【００７７】したがって、本実施形態１の階調電圧生成回路を使用するこにより、高画質で低消費電力の液晶表示装置を構成することが可能となる。

【００７８】〔実施形態２〕図４、図５は、本発明の他の実施形態（実施形態２）である液晶表示装置のドレインドライバの階調電圧生成回路を示す図である。

【００７９】一般に図１４に示す電圧透過率特性は液晶層の材料によって異なる。

【００８０】従って電源回路１３の階調基準電圧は液晶層の電圧透過率特性に合わせて設定され、ドレインドライバ１１内の階調電圧生成回路も電圧透過率特性に合わせて設定しなければならないので、ドレインドライバ１１の汎用性がなく、各液晶表示パネル毎に専用のドレインドライバ１１を用いなければならず、液晶表示装置のコストが高くなる問題がある。

【００８１】本実施形態２は、前記実施形態１をより具体的にした実施形態であり、液晶表示パネルに合わせて容易にドレインドライバ１１の階調電圧生成回路の階調電圧の設定値を変更可能にした実施形態である。

【００８２】本実施形態２の階調基準電圧生成回路では、半導体製造段階において図４に示すように、各階調基準電圧（Ｖ１～Ｖ７）の階調基準電圧印加端子を、直列抵抗分圧回路１のいくつかの点（Ａ、Ｂ、Ｃ）へヒューズ３２を介して接続する。

【００８３】この場合、Ａ、Ｂ、Ｃの各点は、実際に使用する可能性がある分圧値となるように選択する。

【００８４】本実施形態２の階調基準電圧生成回路を、実際に使用する時に、各階調基準電圧（Ｖ０～Ｖ８）として所定の階調基準電圧を印加すると、各階調基準電圧の電圧差に比例した抵抗値のところに接続されたヒューズ３２には電流が流れず、ヒューズ３２は溶断されない。

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【００８５】しかしながら、それ以外のヒューズ３２には電流が流れ、ヒューズ３２が溶断され、これにより、直列抵抗分圧回路１の各階調基準電圧印加端子間の抵抗値は、各階調基準電圧の電圧差に比例した抵抗値となる。

【００８６】また、図５に示すように、直列抵抗分圧回路１の出力スイッチ３が接続されている側にも、同様に各階調電圧出力端子４をヒューズ２を介して、直列抵抗分圧回路１のいくつかの点（Ｄ、Ｅ、Ｆ）へ接続する。

【００８７】表示用データに基づき、所定階調、例えば、階調Ｖ６２を選択した後、階調基準電圧Ｖ８，Ｖ７の階調基準電圧印加端子と階調電圧出力端子４に所定の電圧を印加する。

【００８８】このとき、階調電圧出力端子４には溶断したくないヒューズ２が接続されている点の抵抗値、例えば、Ｅの点に対応した電圧（０．８×Ｖ８（７））を印加する。

【００８９】このように、本実施形態２の階調電圧生成回路では、出力スイッチ３が接続されている側のヒューズ２を溶断するときには、各階調基準電圧の電圧差のみ実使用時に対応した値とし、絶対値は実使用時より高い電圧とする。

【００９０】これにより、本実施形態２の階調電圧生成回路では、実使用時にヒューズ２が溶断されない電流を流すことができる。

【００９１】以上説明したように、本実施形態２では、ドレインドライバ１１に汎用性を持たせることが出来、前記実施形態１と同様、高画質で低消費電力である液晶表示装置を様々な液晶表示パネルの特性に対応して、容易に実現することが可能となる。

【００９２】〔実施形態３〕図６は、本発明の他の実施形態（実施形態３）である液晶表示装置のドレインドライバの階調電圧生成回路を示す図である。

【００９３】本実施形態３も、前記実施形態１をより具体的にした実施形態であり、液晶表示パネルに合わせて容易にドレインドライバ１１の階調電圧生成回路の階調電圧の設定値を変更可能にした実施形態である。

【００９４】本実施形態３の階調電圧生成回路は、直列抵抗分圧回路１の各階調基準電圧（Ｖ０－Ｖ８）の階調基準電圧印加端子間に、何種類かの複数の直列抵抗回路（１０１，１０２，１０３）を設けておき、実使用時に、各階調基準電圧の電圧差の比に近い抵抗比となる直列抵抗回路（１０１，１０２，１０３）を、切替え信号により選択する。

【００９５】また、同じく、切替え信号により切替えスイッチ５を切り替えて、各直列抵抗回路（１０１，１０２，１０３）からの階調電圧を各階調電圧出力端子４に出力するようにしたものである。

【００９６】このとき切替え信号は、表示制御装置１０内のレジスタ、ＥＰＲＯＭ、あるいはコンピュータと接

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続するインタフェースコネクタの専用の入力端子等から各ドレインドライバ１１に供給されるようにしておく。

【００９７】これにより、実使用時の各階調基準電圧の電圧差の比に近い抵抗比を有する直列抵抗分圧回路を容易に実現でき、本実施形態３の階調電圧生成回路でも、ドレインドライバ１１に汎用性を持たせることが出来、前記実施形態１と同様、高画質で低消費電力である液晶表示装置を様々な液晶表示パネルの特性に対応して、容易に実現することが可能となる。

【００９８】〔実施形態４〕図７は、本発明の他の実施形態（実施形態４）である液晶表示装置のドレインドライバの階調電圧生成回路を示す図である。

【００９９】本実施形態４も、前記実施形態１をより具体的にした実施形態であり、液晶表示パネルに合わせて容易にドレインドライバ１１の階調電圧生成回路の階調電圧の設定値を変更可能にした実施形態である。

【０１００】本実施形態４の階調電圧生成回路でも、前記実施形態３と同様、直列抵抗分圧回路１の各階調基準電圧（Ｖ０－Ｖ８）の階調基準電圧印加端子間に、何種類かの複数の直列抵抗回路（１０１，１０２，１０３）を設けておき、各階調基準電圧の電圧差の比に近い抵抗比となる直列抵抗回路（１０１，１０２，１０３）を、半導体製造工程中の金属配線層等のみの変更により選択する。

【０１０１】また、同じく、半導体製造工程中の金属配線層等のみの変更により切替え手段６を切り替えて、各直列抵抗回路（１０１，１０２，１０３）からの階調電圧を各階調電圧出力端子４に出力するようにしたものである。

【０１０２】これにより、実使用時の各階調基準電圧の電圧差の比に近い抵抗比を有する直列抵抗分圧回路を容易に実現でき、本実施形態４の階調電圧生成回路でも、ドレインドライバ１１に汎用性を持たせることが出来、前記実施形態１と同様、高画質で低消費電力である液晶表示装置を様々な液晶表示パネルの特性に対応して、容易に実現することが可能となる。

【０１０３】なお、前記各実施形態では、液晶表示装置に本発明を適用した場合について説明したが、これに限定されず、本発明は、液晶表示モジュール等のすべての液晶表示装置に適用できることはいうまでもない。

【０１０４】以上、本発明を実施形態に基づき具体的に説明したが、本発明は、前記実施形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更し得ることは言うまでもない。

【０１０５】

【発明の効果】本願において開示される発明のうち代表的なものによって得られる効果を簡単に説明すれば下記の通りである。

【０１０６】（１）本発明によれば、液晶層に印加する多階調の階調電圧を生成する液晶表示装置の階調電圧生

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成回路において、直列抵抗分圧回路１の各階調基準電圧印加端子間の抵抗値が、各階調基準電圧間の電圧差に比例しており、直列抵抗分圧回路の階調基準電圧印加端子のうちで、最大の階調基準電圧と最小の階調基準電圧電圧とが印加される階調基準電圧印加端子以外からの電流の流入、流出はほとんど０となり、ドレインドレイバの消費電力を低減することが可能となり、これにより、液晶表示装置の消費電力を低減することが可能となる。

【０１０７】（２）本発明によれば、印加電圧に対する液晶層の透過率の変化が大きい中間調表示の部分では、階調基準電圧印加端子間の抵抗値が小さいため、同一階調電圧を出力するドレイン信号線の本数が多くなっても、階調基準電圧生成回路の階調電圧の電圧変動が小さくなり、異なるドレインドライバ１１間で表示画面の輝度差の発生を抑えることが可能となる。

【図面の簡単な説明】

【図１】本発明の一実施形態（実施形態１）である液晶表示装置のドレインドレイバの階調電圧生成回路を示す図である。

【図２】本発明の一実施形態（実施形態１）である液晶表示装置のドレインドレイバの階調電圧生成回路に具体的な抵抗値及び階調基準電圧値を当てはめた図である。

【図３】図２に示した階調基準電圧と液晶表示素子の透過率との関係を示す図である。

【図４】本発明の他の実施形態（実施形態２）である液晶表示装置のドレインドレイバの階調電圧生成回路を示す図である。

【図５】本発明の他の実施形態（実施形態２）である液晶表示装置のドレインドレイバの階調電圧生成回路を示す図である。

【図６】本発明の他の実施形態（実施形態３）である液晶表示装置のドレインドレイバの階調電圧生成回路を示す図である。

【図７】本発明の他の実施形態（実施形態４）である液晶表示装置のドレインドレイバの階調電圧生成回路を示す図である。

【図８】ＴＦＴ液晶表示装置の概略構成を示すブロック図である。

【図９】ＴＦＴ液晶表示装置の画素の等価回路を示す図である。

【図１０】ＴＦＴ液晶表示装置の画素に印加する電圧のタイミング関係を示す図である。

【図１１】ドレインドライバの概略構成を示すブロック図である。

【図１２】従来のドレインドライバ１１の階調電圧生成回路を示す図である。

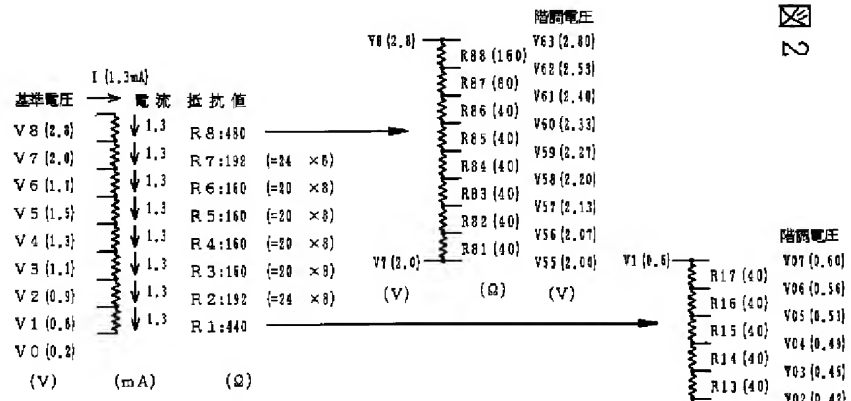
【図１３】電源回路の階調基準電圧生成部の回路図である。

【図１４】図１１に示した、階調基準電圧と液晶表示素子の透過率との関係を示す図である。

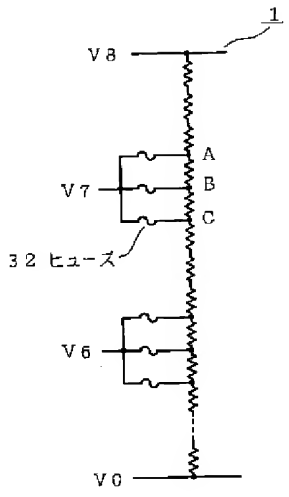
【符号の説明】

ＴＦＴ－ＬＣＤ…ＴＦＴ液晶表示パネル、１…直列抵抗分圧回路、２，３２…ヒューズ、３…スイッチ、４…階調電圧出力端子、５…切替えスイッチ、６，７…切替え手段、１０…表示制御装置、１１…ドレインドライバ、１２…ゲートドライバ、１３…電源回路、１０１，１０２，１０３…直列抵抗回路。

【図２】

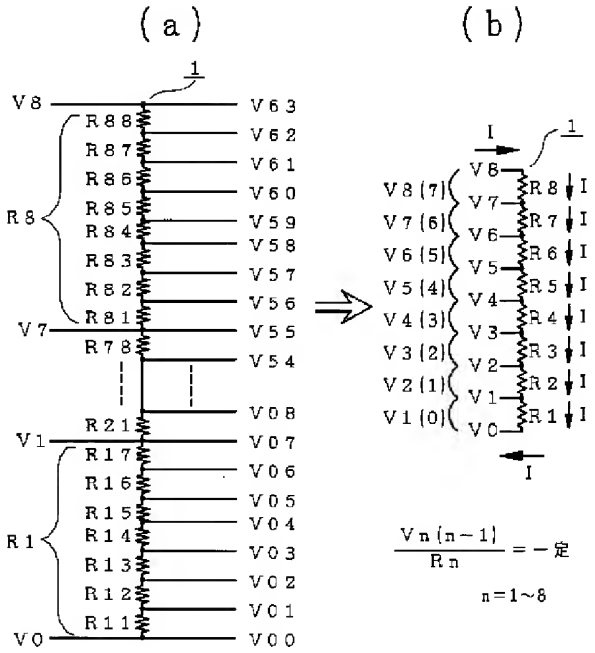


【図４】



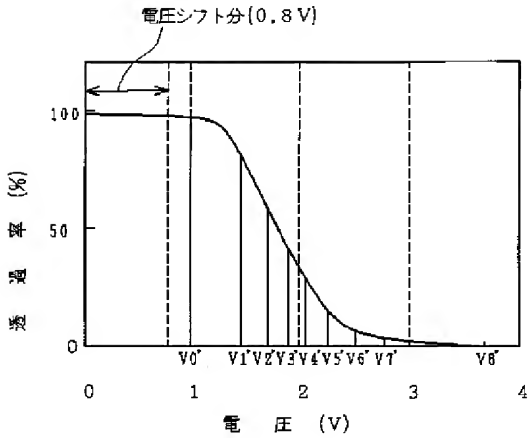
【図１】

図１



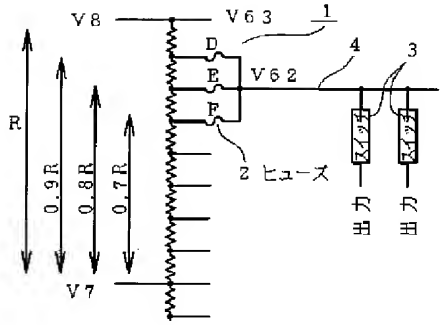
【図３】

図３



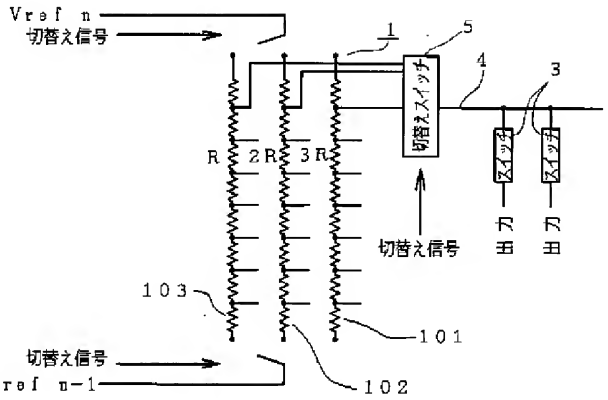
【図５】

図５



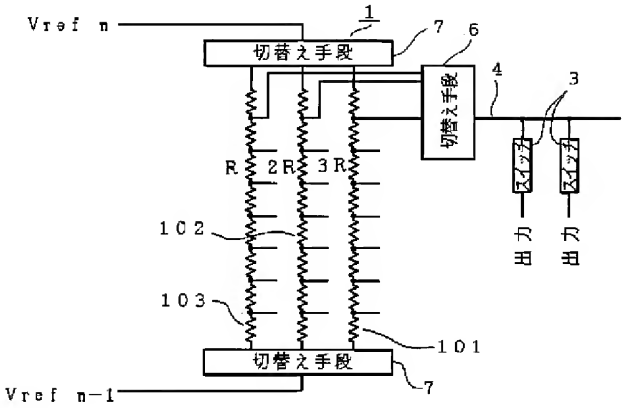
【図６】

図６



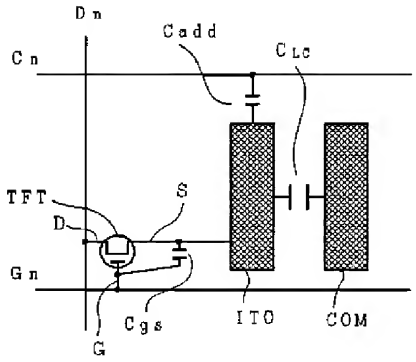
【図７】

図７



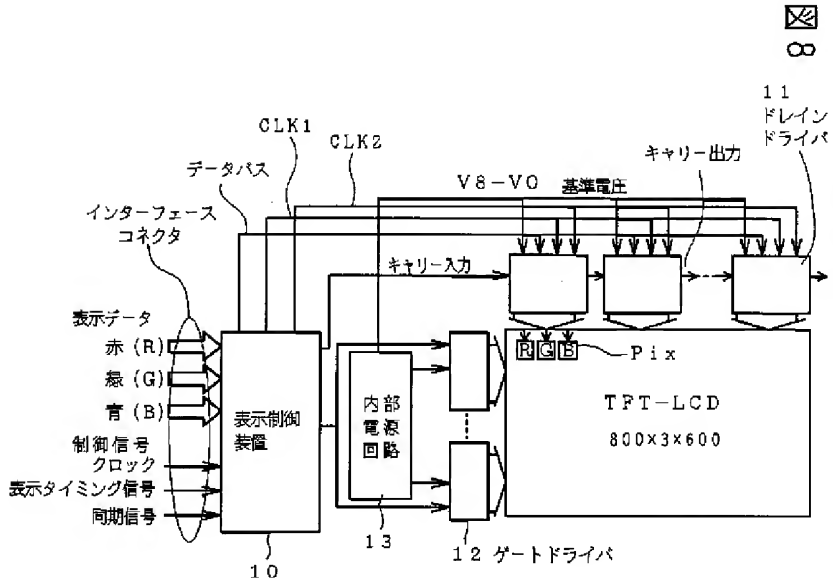
【図９】

図９



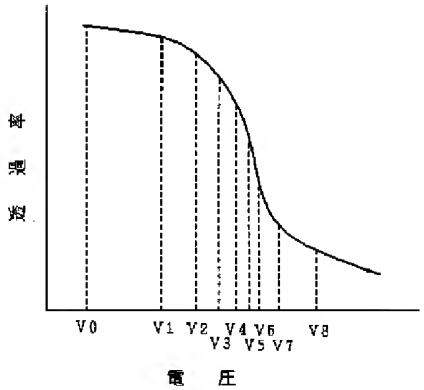
【図８】

図８



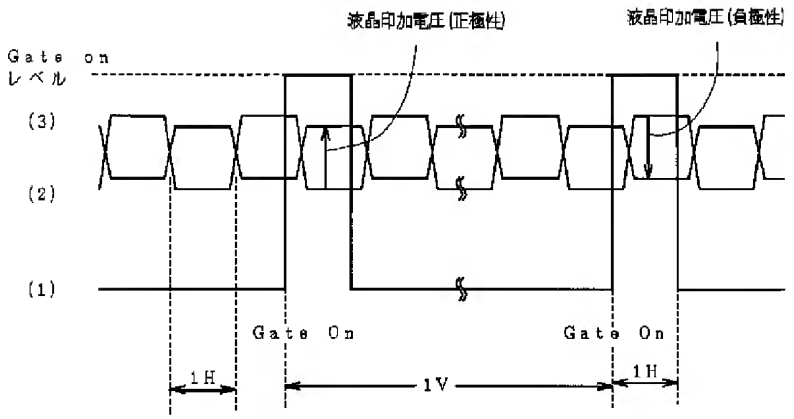
【図１４】

図１４



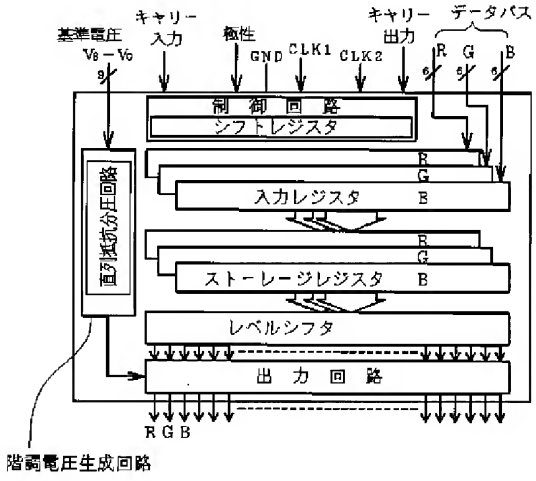
【図１０】

図１０



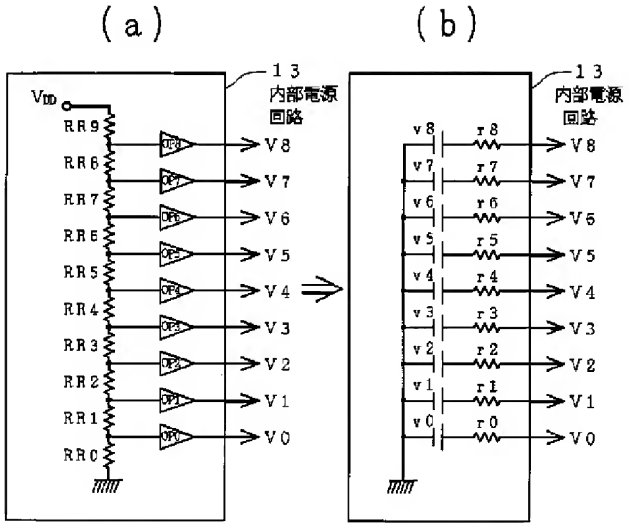
【図１１】

図１１



【図１３】

図１３



【図１２】

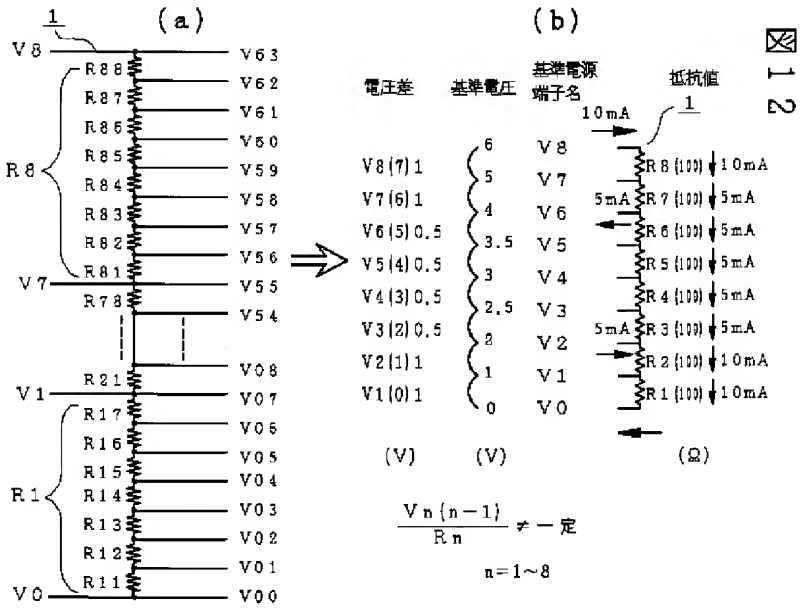


図１２

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